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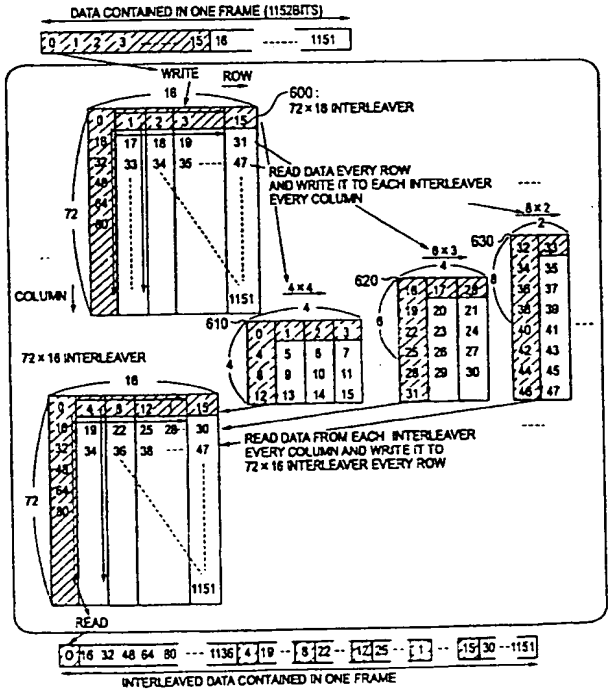
(54) INTERLEAVING METHOD, INTERLEAVING APPARATUS, AND RECORDING MEDIUM IN WHICH INTERLEAVE PATTERN GENERATING PROGRAM IS RECORDED

(57) Data of an input data series is written into a first interleaver. The data is read out column by column or row by row from the first interleaver and written into a plurality of second interleavers column by column or row by row. The data is read from each of the second interleavers and written into one or a plurality of third interleavers as necessary. The operation is repeated once or a plurality of times, thereby reading the data from each of the interleavers and generating a data series. Interleaving is carried out by generating interleaving patterns with a plurality of interleaving patterns. Further, an interleaving pattern suitable for turbo encoding or transmission is generated.

FIG. 6



EP 0 952 673 A1

Description

TECHNICAL FIELD

[0001] The present invention generally relates to an interleaving technology for improving error correction ability of an error correction code for burst error. More particularly, the present invention relates to an interleaving method, an interleaving device, and a medium which stores an interleaving pattern generating program for improving the effect of the interleaving by increasing the degree of data randomizing.

BACKGROUND ART

[0002] In digital transmissions of such as a mobile communications system, the level of received signals varies largely over time by a multipath fading caused by reflections from a building and the like. Therefore, a digital error, such as a burst error, may occur. In addition, in a storing medium of digital systems, such as a compact disc or a hard disk, a digital error such as a burst error may occur due to a scratch, dust or the like on the reading surface of the medium. Thus, various error correction codes are used by various systems. In such an error correction code, for improving the correction ability with respect to the burst error, an interleaving technology is used in concert with the error correction code. The correction ability of the error correction code when a burst error exists depends on the interleaving technology.

[0003] In addition, a turbo encoder which uses a high-ability error correction code which has been proposed in recent years includes a plurality of encoders, and each encoder is connected to each other through an interleaver (which carries out interleaving processing), for decreasing the degree of correlation of redundancy system between the encoders. The interleaver is very important for determining the ability of the turbo code.

[0004] Therefore, an interleaving method applicable for turbo encoding and transmission systems such as the above-mentioned mobile communication systems using the above mentioned interleaver are required.

[0005] As is well known to a person skilled in the art, the purpose of the interleaving method is to randomize the bit sequence of an input bit series and the bit sequence of an output bit series. The following viewpoint can be used as criteria for evaluating the ability of the interleaving method.

(1)How far apart two successive input bits can be separated in the output series.
(2)How far apart two successive output bits are separated in the input series.

[0006] Fig.1 shows a block interleaving method as a conventional interleaving method.

[0007] As shown in Fig.1, data 100 of one frame includes 1152 bits. A matrix 110 has a buffer of N × M (N rows and M columns). The interleaving method is realized such that M bit data is written in the direction of the row, for example, like a vector 115 shown as a diagonally shaded area A, and N bit data is read out in the direction of the column shown as a diagonally shaded area B. By evaluating the interleaving method in terms of the above mentioned criteria, it is recognized that

(1) two successive input bits can not be separated farther apart than N bits in an interleaved output series 130, and
(2) two successive output bits are separated as far apart as at least M bits in the input series.

[0008] However, in the above-mentioned interleaving method, an input bit series is written in the row direction in order of time in the input bit series, and the written data is read out in the column direction also in order of time in the input bit series. Therefore, data is written/read only once in order of time in each of the processes. Therefore, the effect of the interleaving is low, and the performance of the randomizing is limited to the above-mentioned degree even with the N×M buffer.

DISCLOSURE OF THE INVENTION

[0009] The present invention is achieved in view of the above-mentioned points. A first objective of the present invention is to provide an interleaving method for improving the effect of the interleaving, comparing with the case of reading and writing one by one in order of time, by applying a process of changing a sequence repeatedly after carrying out a process of reading or writing to a buffer once.

[0010] To achieve the above-mentioned objective, according to the present invention, an interleaving method for inputting a data series of a unit length and outputting an interleaved series of the unit length, includes:

a first step of writing data of the data series to a first interleaver, reading out the data column by column or row by row from the first interleaver, and writing the data to a plurality of second interleavers;

a second step of reading out the data from each of the second interleavers, and writing the data to one or a plurality of third interleavers as necessary, and

reading out the data from each of interleavers generated by repeating the second step once or a plurality of times or from each of interleavers generated by the first step, and outputting a data series.

[0011] The above-mentioned invention may be configured such that an interleaving method for inputting a data series of a unit length and outputting an interleaved series of the unit length, includes:

a first step of writing the data series to a first interleaver in one direction;
a second step of reading out column data or row data from the first interleaver, writing the read out data to a second interleaver, which has a size different from a size of the first interleaver, in one direction, and repeating the reading out column data or row data and the writing the read out data column by column or row by row;
repeating a third step of performing the second step wherein each of a plurality of the second interleavers generated by the second step is regarded as the first interleaver, and
reading out data from each of interleavers generated by repeating the third step or by performing the second step, and outputting a data series.

[0012] The above-mentioned interleaving method may be configured such that an interleaving method for inputting a data series of a unit length and outputting an interleaved series of the unit length, includes:

a first step of writing the data series to a first interleaver in one direction;
a second step of reading out column data or row data from the first interleaver, writing the read out data to a second interleaver, which has a size different from a size of the first interleaver, in one direction, and repeating the reading out column data or row data and the writing the read out data column by column or row by row;
a third step of reading out data column by column or row by row from each of interleavers generated by the second step, and writing the data to an interleaver which has a size the same as the size of the first interleaver, and
reading out data from the interleaver generated by the third step, and outputting a data series.

[0013] In the above configuration, the interleaving method includes:

a fourth step of performing the second step and the third step wherein the interleaver generated by the third step is regarded as the first interleaver, reading out data from an interleaver generated by repeating the fourth step once or a plurality of times, and outputting a data series.

[0014] The interleaving method may be configured such that an interleaving method for inputting a data series of a unit length and outputting an interleaved data series of the unit length, includes:

storing a plurality of interleaving patterns in a table beforehand;
applying one of the interleaving patterns to the input data series by referring to the table and outputting data, and
repeating a step of applying one of the interleaving patterns to the output data, and outputting the interleaved data series.

[0015] In the above mentioned configuration, an interleaving pattern is stored in the table according to the interleaving method as claimed in one of claims 1 - 4.

[0016] According to the above mentioned invention, because a process of changing sequence is applied repeatedly after carrying out a process of reading or writing to a buffer once, the effect of interleaving can be improved comparing with the case of reading and writing one by one in order of time.

[0017] The second objective of the present invention is to provide an interleaving method for supporting various interleaving flexibly with decreased data amount necessary for the interleaving.

[0018] To achieve the above mentioned objectives, according to the present invention, a method for generating an interleaving pattern description of an interleaving pattern for interleaving an input data series of a unit length and outputting an interleaved data series of the unit length, includes:

generating the interleaving pattern description of a third unit by using an interleaving pattern description of a first unit and an interleaving pattern description of a second unit.

[0019] The present invention generates an interleaving pattern description of a predetermined length unit by using the interleaving pattern description generation method as claimed in claim 7.

[0020] In the above configuration, the interleaving pattern description is an interleaving pattern table or an interleaving pattern equation which describes an interleaving pattern.

[0021] The interleaving method of the present invention may be configured such that an interleaving method for inputting a data series of a unit length and outputting an interleaved data series of the unit length, includes:

generating an interleaving pattern description of a third unit by using an interleaving pattern description of a first unit and an interleaving pattern description of a second unit, and
interleaving with the generated interleaving pattern description.

[0022] Further, the interleaving method of the present invention may be configured such that an interleaving method for inputting a data series of a unit length and outputting an interleaved data series of the unit length, includes:

calculating interleaving destinations in a series of a third unit with an interleaving pattern description of a first unit and an interleaving pattern description of a second unit, and
interleaving with the result of the calculation.

[0023] Further, the interleaving method includes:

generating an interleaving pattern description of a first unit and an interleaving pattern description of a second unit by using the interleaving pattern description generated by the method,
interleaving a data series of a third unit by calculating from the interleaving pattern description of a first unit and the interleaving pattern description of a second unit.

[0024] Further, that the interleaving pattern description is an interleaving pattern table or an interleaving pattern equation which describes an interleaving pattern.

[0025] According to the above mentioned present invention, by generating the interleaving pattern description, for example, from one interleaving pattern table (in the case of A=B), or from two interleaving pattern tables, an interleaving pattern table which has a larger interleaving length can be generated. Thus, a pattern of a certain interleaving length can be represented by a combination of a plurality of patterns of smaller interleaving lengths. Therefore, memory amount for fixed length patterns can be decreased. For example, conventionally, in the case of using an interleaving pattern table for 1000 bits, a memory for 1000 bits is necessary. According to the present invention, by representing the interleaving pattern table for 1000 bits with a 20 bit interleaving pattern table and a 50 bit interleaving pattern table, the memory can be decreased to an amount for 70 (=20 + 50) bits. In addition, by representing an interleaving pattern table 900 bits with a 20 bit interleaving pattern table × a 50 bit interleaving pattern table, interleaving for 1000 bits and 900 bits are possible without enlarging the fixed length interleaving pattern table.

[0026] A method according to the present invention may be configured such that a method for generating an interleaving pattern description of an interleaving pattern for interleaving an input data series of a unit length and outputting an interleaved data series of the unit length, includes:

interpreting an interleaving pattern description language which defines an interleaving pattern, and
generating an interleaving pattern description by using the method as claimed in claim 9 on the basis of the interpretation.

[0027] In the above configuration, if an interleaving pattern description corresponding to a part of the interleaving pattern description language is stored, the interleaving pattern description is generated with reference to the stored interleaving pattern description without performing a process corresponding to the part of the interleaving pattern description language, when generating an interleaving pattern.

[0028] Further, the interleaving method includes:

interpreting an interleaving pattern description language which defines an interleaving pattern, and
interleaving by the method as claimed in claim 13 on the basis of the interpretation.

[0029] In the above configured interleaving method, if an interleaving pattern description corresponding to a part of the interleaving pattern description language is stored, the interleaving pattern description is generated with reference to the stored interleaving pattern without performing a process corresponding to the part of the interleaving pattern description language, when interleaving.

[0030] The present invention may be configured such that a method for generating an interleaving pattern description of an interleaving pattern for interleaving an input data series of a unit length and outputting an interleaved data series

of the unit length, includes:

determining an interleaving pattern description of a first stage when a unit length is given, and
generating an interleaving pattern description by repeating a process of determining interleaving patterns corresponding to interleavers of a column and a row of a stage after the first stage until reaching any stage or until becoming unable to interleave.

[0031] Further, the present invention may be configured such that a method for generating an interleaving pattern description of an interleaving pattern for interleaving an input data series of a unit length and outputting an interleaved data series of the unit length, includes:

checking an interleaving pattern description which is generated;
generating an interleaving pattern description again after changing all or a part of parameters if the result of the checking is unsuccessful, and
repeating the checking and the generation until the result of the checking becomes successful so as to generate an interleaving pattern description which passed the checking.

[0032] In the above configured interleaving pattern description generation method, the interleaving pattern description which is generated is an interleaving pattern table or an interleaving pattern equation or an interleaving pattern description language.

[0033] According to the above mentioned present invention, various interleaving can be supported flexibly with decreased data amount necessary for the interleaving.

[0034] The third objective of the present invention is to provide a method for applying the interleaving method to a transmission system device, a turbo encoder, or the like, and to provide the devices such as the transmission system device and the encoder, and a medium storing an interleaving pattern generating program suitable for a target.

[0035] To achieve the above objectives, the present invention may be configured such that a method for generating an interleaving pattern description of an interleaving pattern for interleaving an input data series of a unit length and outputting an interleaved data series of the unit length, includes:

a step of determining, when a unit length is given, the number of rows or columns of a block interleaver corresponding to the unit length by using an interleaving pattern list suitable for a predefined application target and defining the number of columns or rows from the determined number of rows or columns, and
generating an interleaving pattern of the unit length from interleaving patterns obtained by repeating the step until the defined number of columns or the defined number of rows is defined in the interleaving pattern list.

[0036] In the above configuration, the method includes:

a first step, which is a process of a first stage, of determining the number of rows or the number of columns of a block interleaver corresponding to a unit length which is given beforehand by a defined number, assuming an interleaving pattern corresponding the defined number as a predefined interleaving pattern, and defining the number of rows by using the determined number of columns or defining the number of columns by using the determined number of rows;
a second step of determining the number of rows or the number of columns of a block interleaver corresponding to the defined number of rows or the defined number of columns by using an interleaving pattern list suitable for predefined application target, and defining the number of columns from the determined number of rows or defining the number of rows from the determined number of columns;
a third step of repeating the second step until an interleaving pattern corresponding to the number of rows or columns exists in the predefined interleaving pattern list;
performing the third step a number of times equal to the number of rows or columns corresponding to the predefined interleaving pattern in the first step, and
generating an interleaving pattern corresponding to the row or the column of a former stage sequentially from an interleaving pattern corresponding to the row and the column which is generated in a final stage.

[0037] Further, in the above configuration, the generated interleaving pattern of the unit length is checked and an interleaving pattern of the unit length is generated again according to the result of the checking.

[0038] Further, in the above configuration, the application target is turbo code and the number of rows of the first stage is 7.

[0039] Further, in the above configuration, the application target is transmission and the number of columns of the

first stage is the number of slots of one frame.

[0040] According to the above mentioned invention, an interleaving pattern suitable for turbo encoding and a transmission system, and the like.

[0041] To achieve the above mentioned objectives, an interleaving device for inputting a data series of a unit length and outputting interleaved data series of the unit length, includes:

means which stores one or a plurality of interleaving patterns in a table beforehand;
means which outputs data by applying one of the plurality of interleaving patterns, and
means which outputs the output data by further applying one of the plurality of interleaving patterns as necessary.

[0042] In the above configuration, the table stores an interleaving pattern by the interleaving method as claimed in one of claims 1 - 4.

[0043] Further, in the above configuration, the interleaving pattern is generated by the interleaving pattern generating method as claimed in claim 21.

[0044] Further, in the interleaving device, interleaving destinations of an input data series are calculated, and the interleaving is performed on the basis of the calculation and data is output instead of using an interleaving pattern.

[0045] According to the above mentioned invention, a device for carrying out interleaving processes can be provided, particularly, a device suitable for turbo encoding and transmission, and the like.

[0046] To achieve the above mentioned objectives, according to the present invention, a computer readable medium storing a program for description and generation of an interleaving pattern in an interleaving method for inputting a data series of a unit length and outputting an interleaved series of the unit length, includes:

a step of determining the number of rows or columns of a block interleaver corresponding to a unit length which is given beforehand by using an interleaving pattern list suitable for a predefined application target and defining the number of columns from the determined number of rows or the number of rows from the determined number of columns, and
generating an interleaving pattern of the unit length from interleaving patterns obtained by repeating the step until the defined number of columns or the defined number of row is defined in the interleaving pattern list.

[0047] Further, in the above configuration, the program includes:

a first step, which is a process of a first stage, of determining the number of rows or the number of columns of a block interleaver corresponding to a unit length which is given beforehand by a defined number, assuming an interleaving pattern corresponding the defined number as a predefined interleaving pattern, and defining the number of rows by using the determined number of columns or defining the number of columns by using the determined number of rows;
a second step of determining the number of rows or the number of columns of a block interleaver corresponding to the defined number of rows or the defined number of columns by using an interleaving pattern list suitable for a predefined application target, and defining the number of columns from the determined number of rows or defining the number of rows from the determined number of columns;
a third step of repeating the second step until an interleaving pattern corresponding to the number of rows or columns exists in the predefined interleaving pattern list;
performing the third step a number of times equal to the number of rows or columns corresponding to the predefined interleaving pattern in the first step, and
generating an interleaving pattern corresponding to the row or the column of a former stage sequentially from an interleaving pattern corresponding to the row and the column which is generated in a final stage.

[0048] In the above configuration, in the computer readable medium storing a program for generation of an interleaving pattern of the present invention, the generated interleaving pattern of the unit length is checked and an interleaving pattern of the unit length is generated again according to the result of the checking.

[0049] Further, in the computer readable medium storing a program for generation of an interleaving pattern of the present invention, the application target is turbo code and the number of rows of the first stage is 7.

[0050] Further, in the computer readable medium storing a program for generation of an interleaving pattern of the present invention, the application target is transmission and the number of columns of the first stage is the number of slots of one frame.

[0051] According to the above mentioned invention, a medium storing a program for generating an interleaving pattern can be provided, particularly, a medium storing a program for generating an interleaving pattern suitable for turbo encoding, transmission and the like can be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

[0052]

Fig.1 is a diagram showing a conventional interleaving method.
Fig.2 is a diagram showing an interleaving method according to a first embodiment of the present invention.
Fig.3 is a diagram showing the interleaving method according to the first embodiment of the present invention.
Fig.4 is a diagram showing the interleaving method according to a second embodiment of the present invention.
Fig.5 is a diagram showing the interleaving method according to a third embodiment of the present invention.
Fig.6 is a diagram showing the interleaving method according to a fourth embodiment of the present invention.
Fig.7 is a diagram showing the interleaving method according to a fifth embodiment of the present invention.
Fig.8 is a diagram showing that L=64-bit length data is written in a block interleaver of 8 bits × 8 bits.
Fig.9 is a diagram showing a first case of interleaving by a symbol unit.
Fig. 10 is a diagram showing a second case of interleaving by a symbol unit.
Fig.11 is a diagram showing a third case of interleaving by a symbol unit.
Fig.12 is a diagram for explaining an interleaving process.
Fig.13 is a diagram for explaining an interleaving process according to a seventh embodiment of the present invention.
Fig.14 is a diagram for explaining an interleaving process according to the seventh embodiment of the present invention.
Fig.15 is a diagram for explaining an interleaving process according to the seventh embodiment of the present invention.
Fig.16 is a diagram for explaining an interleaving process according to an eighth embodiment of the present invention.
Fig.17 is a diagram for explaining an interleaving process according to the eighth embodiment of the present invention.
Fig.18 is a diagram for explaining an interleaving process according to a ninth embodiment of the present invention.
Fig.19 is a diagram for explaining an interleaving process according to the ninth embodiment of the present invention.
Fig.20 is a diagram for explaining an interleaving process according to the ninth embodiment of the present invention.
Fig.21 is a diagram for explaining an interleaving process according to the ninth embodiment of the present invention.
Fig.22 is a diagram for explaining an interleaving process according to the ninth embodiment of the present invention.
Fig.23 is a diagram for explaining an example of definition of an interleaving pattern description language.
Fig.24 is a diagram for explaining an example of definition of the interleaving pattern description language.
Fig.25 is a diagram for explaining an example of definition of the interleaving pattern description language.
Fig.26 is a diagram for explaining an example of definition of the interleaving pattern description language.
Fig.27 is a diagram for explaining an example of realizing interleaving in the case of using the interleaving pattern description language.
Fig.28 is a diagram for explaining an example of realizing interleaving in the case of using the interleaving pattern description language.
Fig.29 is a diagram for explaining an example of realizing interleaving in the case of using the interleaving pattern description language.
Fig.30 is a diagram for explaining an example of realizing interleaving in the case of using the interleaving pattern description language.
Fig.31 is a diagram for explaining an example of realizing interleaving in the case of using the interleaving pattern description language.
Fig.32 is a diagram showing a process flow for generating an interleaving pattern.
Fig.33 is a flowchart showing a process for determining the generated interleaving pattern.
Fig.34 is a block diagram for explaining an example of a configuration of a turbo encoder.
Fig.35 is a block diagram for explaining an example of a configuration of a mobile radio transmitter-receiver.
Fig.36 is a diagram showing an example of deinterleaving.
Fig.37 is a diagram showing an example of deinterleaving.
Fig.38 is a flowchart for explaining generation of an interleaving pattern suitable for turbo code.
Fig.39 is a diagram showing details of the determining process of the interleaving pattern.
Fig.40 is a table showing a list of predetermined interleaving patterns used for the determining process of the inter-

leaving pattern.

Fig.41 is a diagram showing details of a generation process of an interleaving pattern by a multistage interleaving method.

Fig.42 is a diagram for explaining a first stage of the generation process of the interleaving pattern.

Fig.43 shows a specific example of the generation process shown in Fig.42.

Fig.44 is a diagram for explaining another example of the generation process of the interleaving pattern.

Fig.45 is a diagram for explaining a check of the generated interleaving pattern.

Fig.46 is a flowchart for explaining a generation process of the interleaving pattern suitable for a transmission line interleaver.

Fig.47 is a diagram showing details of a determining process of the interleaving pattern.

Fig.48 is a table showing a list of the predetermined interleaving patterns used for generating an interleaving pattern.

Fig.49 is a diagram showing details of a generation process of an interleaving pattern by a multistage interleaving method.

Fig.50 is a diagram showing an example of a device for interleaving.

PREFERRED EMBODIMENTS FOR CARRYING OUT THE INVENTION

[0053] In the following, a detailed description of embodiments of the present invention will be given with reference to figures. Although an interleaver is described as a two-dimensional array in the figures in the following description, it is only as a matter of convenience. It is needless to say that the present invention can be carried out with a one-dimensional array instead of the two-dimensional array.

[0054] The interleaving processes described in the following are carried out by a processing device for signal processing of an input bit series and the like.

[0055] First, a first embodiment of the present invention will be described.

[0056] Fig.2 and Fig.3 show the interleaving method of the first embodiment of the present invention. As shown in Fig.2, 1152-bit data as single frame data 200 is input, as in the case of the conventional method, and a row vector 215 is written to a buffer of an interleaver 210 of 72×16 (=1152) in the direction of the row. It is needless to say that the interleaving method of the present invention can be applied to a general N×M interleaver instead of the 72×16 interleaver. In the 72×16 interleaver 210, each of 16 column vectors, including a vector 220 which has 72 bits, is read out, and is interleaved by a 9×8 (=72) interleaver 230, 235, • • •, or 240 which corresponds to each of 16 column vectors. That is to say, for example, the column vector 220 is written in the buffer of the 9×8 (=72) interleaver 230 in the direction of the row. Finally, data in each of the 16 9×8 interleavers is read out in the direction of the column successively, and, then, the interleaved data 245 is output, in other words, extracted.

[0057] The interleaved data shown in Fig.1 is arranged orderly in order of time in terms of the column part. In contrast, the data arrangement in Fig.2 is more complex. Here, to evaluate quantitatively the performance of the interleaving, the performance of the interleaving is evaluated from the viewpoint of the criterion (2) described in the related art.

[0058] In the output 130 in Fig.1, the number adjacent to "0" is "16". Therefore, in the input data, the two bits are separated by at least 16 bits. When all bits are examined, it is recognized that two successive bits of output are separated by at least 16 bits in the input series. That is to say, the above-mentioned evaluation according to the criterion (2) is 16 bits.

[0059] The result of an evaluation according to the criterion (2) of the method shown in Fig.2 is 128 bits. Therefore, it is understood that the performance of interleaving is improved.

[0060] Fig.3 shows a method in which an additional interleaving is performed. As shown in Fig.3, each column data in each of the 9×8 interleavers such as the interleaver 230 shown in Fig.2 is interleaved by each of 3×3 (=9) block interleavers. At the end stage of the interleaving, interleaved data 295 is output or extracted by reading out data sequentially in the column direction from the 3×3 block interleavers such as the interleaver 285.

[0061] According to the method shown in Fig.3, since the result of the evaluation by the above-mentioned criterion (2) is 384 bits, it can be understood that the performance of interleaving will improve by repeating the interleaving process.

[0062] In the following, a second embodiment of the present invention will be described. Fig.4 shows an interleaving method according to the second embodiment of the present invention.

[0063] Different from the method shown in Fig.3 in which data, in the 72×16 interleaver 210 is read in the column direction, in the method according to the second embodiment, 16 bits in row vectors in an 72×16 interleaver 310 are read and written to each of 4×4 interleavers such as an interleaver 320 in the row direction. Next, each column of each of the 4×4 interleavers such as the interleaver 320 is read in the column direction sequentially and is written back to each row in the 72×16 interleaver 310. In this case, another interleaver 335 can be used instead of the 72×16 interleaver 310. After all data in the 4×4 interleavers are written back to the 72×16 interleaver 310, interleaved data 340 is extracted by reading a buffer of the 72×16 interleaver 310 in the column direction.

[0064] Compared with the output result 350 according to the conventional interleaving method, data alignment in each column in the 72x16 interleaver 310 is the same as that of the conventional method, however, it can be recognized that column alignment is different. This interleaving method will be evaluated from the viewpoint of the criterion (1) in the following. According to the conventional method, the input data "0" and "1" are interleaved to be 72 bits apart. Similarly evaluating all bits in terms of the criterion (1), the result is 72 bits. In the second embodiment, since the result is 288 bits, it can be understood that the performance of the interleaving is improved.

[0065] In the following, a third embodiment of the present invention will be described. Fig.5 shows an interleaving method of the third embodiment of the present invention. The embodiment is a method in which methods of the first and second embodiments are utilized in combination and each of the interleaving methods is repeated.

[0066] In Fig.5, single frame data 400 of 16 bits is input and written to a buffer of a 4 × 4 (=16) interleaver 410 in the row direction. Each of the 4 columns consists of 4 bits and is interleaved by one of four 2 × 2 (=4) interleavers 420, 425, 430, 435 as shown in Fig.5. That is, each of the columns is written into the buffer of the 2 × 2 (=4) interleavers such as the interleaver 420 in the row direction.

[0067] Next, the 2 bits of each column of each 2 × 2 (=4) interleaver are read successively and returned to each column of the 4 × 4 interleaver 410. In this case, another 4 × 4 interleaver 440 can be used instead of the 4 × 4 interleaver 410.

[0068] Each row data is read from the interleaver 410 or 440 and is interleaved by a corresponding one of four 2×2 (=4) interleavers 445, 450, 455, and 460. That is, the row data of the interleaver 410 or 440 is written to the buffer of the 2×2 (=4) interleaver in the row direction.

[0069] Next, 2 bits of each column of every 2×2 interleaver such as the interleaver 445 are successively read and returned to each row of the 4 ×4 interleaver 410 or 440. In this case, another 4 ×4 interleaver 470 can be used instead of the 4×4 interleaver 410 or 440. After all column data of the 2×2 interleavers 445-460 are returned, the buffer of the 4×4 interleaver 410, 440, or 470 is read in the column direction and interleaved data 480 is extracted.

[0070] According to the above-mentioned method, since the performances in terms of the criteria (1) and (2) are improved simultaneously, the interleaving performance can be further improved.

[0071] Therefore, according to the present invention, in an interleaving of an NxM buffer size, two successive input bits can be separated such that the distance between the two bits becomes more than 2N bits in the output series after interleaving is repeated enough times, and two successive two output bits can be separated in the input series such that the distance between the two bits is more than 2M bits. For example, in the case of 8×8 buffer size interleaving, two successive input bits can be separated farther apart than 2×8 bits in the output series after three times of repeated interleaving and two successive output bits can be separated farther apart than 2×8 bits in the input series.

[0072] Further, the present invention can be used for randomization of burst error arising in a burst error transmission line or a burst error recording medium, and also can be used for an interleaving method applied to turbo encoding.

[0073] In the following, a fourth embodiment of the present invention will be described. Fig.6 shows the embodiment.

[0074] It is not necessary to use the same interleavers repeatedly for the same interleaving step as in the above-mentioned first to third embodiments. As shown in Fig.6, after writing an input series to a 72×16 interleaver 600, each row of the interleaver 600 is read by 16 bits. In this case, the interleaver's shape can be varied such that the first row is written to a 4×4 interleaver 610, the second row is written to a 6×3 interleaver 620, and the third row is written to a 8×2 interleaver 630, and the like. It is also not necessary to fill an interleaver buffer with input data, for example, a 6×3 interleaver may be used for the 16-bit input series.

[0075] A fifth embodiment of the present invention will be described in the following. Fig.7 shows the fifth embodiment.

[0076] Fig.7 shows an example of interleaving similar to that shown in Fig.2. In the case of the example shown in Fig.2, an input series is divided into a plurality of 16 bit blocks, wherein the sequence of the bits in each block remains in the same order of time in the first interleaving step. On the other hand, in the case of the example shown in Fig.7, pseudo-random interleaving is performed on each block and the data in the block is written to a 72×16 interleaver 700. Thus, interleaving repeating processes of the present invention can be combined with interchanging processes of a bit sequence such as that used for a pseudo-random interleaving method. Fig.7 shows an example of such an interleaving method.

[0077] Next, a sixth embodiment of the present invention will be described. In the above-mentioned embodiments, interleaving methods by a bit unit are described. Interleaving by a symbol unit is also possible. In the following, the sixth embodiment will be described as an example of the interleaving by a symbol unit.

[0078] First, L-bit length data is written to an NxM (L≦ NxM) block interleaver.

[0079] Here, one symbol will be considered to be K bits hereinafter. That is, in an NxM block interleaver, successive (adjacent) K bits will be considered to be one symbol.

[0080] In a first case in which K successive bits in the vertical direction are assumed to be one symbol, a block interleaver can be considered to be an (N/K) symbol x M symbol block interleaver. Therefore, symbol interleaving is possible by performing multiple stage interleaving in the vertical direction and in the horizontal direction in the way mentioned above and by converting the symbol to bits, which are read out. In a second case in which K bits in the horizontal direc-

tion are assumed to be one symbol, the block interleaver can be considered to be an N symbol × (M/K) symbol block interleaver. Therefore, symbol interleaving is also possible. Further, in a third case in which K adjacent bits are considered to be one symbol where K is N1×M1, the block interleaver can be considered to be an (N/N1) symbol × (M/M1) symbol block interleaver, thereby symbol interleaving is also possible.

[0081] Concrete examples of the above-mentioned methods will be described with reference to figures. Fig.8 shows L=64 bit length data written to an (N=) 8 bit × (M=) 8 bit block interleaver. The following processes will be described with reference to Fig.9 - Fig.11 corresponding the above mentioned first case to third case respectively.

[0082] Fig.9 shows the first case in which K equals 2. A 4 symbol × 8 symbol block interleaver shown in Fig.9 is interleaved in the above-mentioned way of a bit unit, and symbols in an interleaver 650 are converted into bits, thereby an interleaver 660 is generated, and, then, the bits are read out.

[0083] In the second case in which K equals 2, interleaving is performed as shown in Fig.10, and, in the third case in which K equals 4, interleaving is performed as shown in Fig.11. The precise description of these methods will be omitted because it is obvious from these figures and above descriptions.

[0084] As mentioned above, according to the interleaving method in the first to sixth embodiments of the present invention, the aforementioned first objective is achieved. That is, by applying an interchanging process on a data sequence repeatedly after writing to or reading from a buffer once, the performance of interleaving will improve as compared with the conventional method in which reading and writing is performed in order of time one by one.

[0085] The interleaving method of the present invention will be called a multiple interleaving method hereinafter.

[0086] As mentioned above, in the case of a digital system, permutation in interleaving is performed by the bit or the symbol. The above-mentioned methods show the way of writing data in a buffer and reading out the data. It is also possible to use a pattern (which will be called an interleaving pattern hereinafter) as sequence permutation information in interleaving which will be referred to when interleaving data. Although, interleaving can be performed by the bit or by the symbol, or the like, an example by the bit will be shown in the following for the sake of simplicity.

[0087] Fig.12 shows an example of interleaving of a 16-bit series. As shown in Fig.12, bit-by-bit interleaving is carried out by referring to an interleaving pattern table. In Fig.12, as for an input 16-bit series 670 which will be interleaved, the sequence of the bits (or the symbols and the like) in the input series are altered according to the sequence stored in the interleaving pattern table 680.

[0088] As shown in Fig.12, the sequence in the interleaving pattern table 680 is read out in order of the vertical direction, as indicated by an arrow, as 0, 8, 4, 12, 2, • • • . Then, the bits of the 16-bit series are interchanged according to the read out sequence such that the 0th bit of the input series is interchanged to the 0th bit of the output series and the first bit is interchanged to the eighth bit and the like. After that, an interleaved bit series is output.

[0089] Next, embodiments of the present invention for achieving the second objectives will be described starting from a seventh embodiment.

[0090] Fig.13 - Fig.15 show the seventh embodiment of the present invention.

[0091] In Fig.13 and Fig.14, an example of interleaving a 16-bit series 670 is shown. That is, an interleaving pattern table A and an interleaving pattern table B, both of which describe a 4 bit series conversion, are provided, and an interleaving pattern table C 680 for 16 (4×4) bit series conversion is generated by the two 4 bit interleaving pattern tables. Then, interleaving of the input 16 bit series 670 is performed with the generated 16 bit series interleaving pattern table.

[0092] In Fig.13, the prepared table A defines the writing direction to the interleaving pattern table C and the table B defines the direction perpendicular to the writing direction. When carrying out interleaving of L=16 bits, the interleaving pattern table C which describes an L (≦LA×LB) bit interleaving pattern is generated by using the interleaving pattern table A which describes an LA=4 bit interleaving pattern and the interleaving pattern table B which describes an LB=4 bit interleaving pattern. (① in Fig. 13)

[0093] According to the example shown in Fig.13, an operation for generating C[i] of the interleaving pattern table which means ith bit of the bit series C is

$$C[i] = A[i\%LA] + LA \times B[i/LA],$$

wherein LA = 4, and i is an address indicating a bit location of the bit series and is an integer equal to or larger than 0. An address indicating a bit location of a series will be represented by one of i, j, k, • • • each of which is an integer equal to or more than 0 hereinafter. A[i] means ith element of the table A. "%" is a modulo operator and "i%LA" means remainder of i divided by LA. "i/LA" means the integer part (in which a fractional portion is dropped) of the result of i divided by LA. The meanings of these operators are the same hereinafter. The table A defines the pattern in a horizontal direction of the table C and the table B defines the pattern in a vertical direction.

[0094] The interleaving pattern table C 680 is generated by writing the result to the interleaving pattern table C 680 in the horizontal direction.

[0095] When interleaving, bits in the table C are read sequentially in the vertical direction and interleaving of the input series is performed by referring to the bits. (② in Fig.13) That is, permutation of the sequence of the bits in the series

is performed according to the sequence stored in the interleaving pattern table C 680.

[0096] In this case, it is not necessary to read out data downward, nor is it necessary to write rightward. Instead, those directions can be reverse to that shown in the figure. For example, reading out may be upward.

[0097] Further, in Fig.13, although it is mentioned that the prepared table A defines the writing direction to an interleaving pattern table C and the table B defines the direction perpendicular to the writing direction, the relationship between table A and B can be interchanged. In addition, the interleaving pattern table A and B can be the same or different patterns.

[0098] If the table A and the table B are the same, it is necessary to use only one of the tables. For example, C[i] can be represented as

$$C[i] = A[i\%LA] + LA \times A[i/LA], \text{ or}$$

$$C[i] = B[i\%LB] + LB \times B[i/LB].$$

These features are the same in Fig.13 - Fig.21.

[0099] Fig.14 shows another operation in which the same result as that shown in Fig.13 can be obtained. The interleaving pattern C 680 in Fig.14 is generated by

$$C[i] = LA \times B[i\%LB] + A[i/LB] \text{ (① in Fig.14)}$$

which is different from the case shown in Fig.13. In this case, the table A defines a pattern of a horizontal direction of the table C, and the table B defines a pattern of a vertical direction of the table C. The result is written to the table C in the vertical direction.

[0100] The relationship between tables A and B can be interchanged. Also, the interleaving pattern tables A and B can be the same or different patterns. If the table A and the table B are the same, it is necessary to use only one of the tables.

[0101] When interleaving, the bits in the table C are read out in the same (vertical) direction sequentially, thereby the input series is interleaved by referring to the bits (② in Fig.14).

[0102] Thus, it is possible to change the operation for the interleaving pattern table C 680. In addition, the reading direction is not necessarily the same as the writing direction, and both directions are not necessarily the same as those shown in Fig.14. That is, the writing direction and reading direction can be set freely.

[0103] Fig.15 shows an example of 15-bit interleaving instead of the 16 bit interleaving shown in Fig.13 or Fig.14.

[0104] As shown in Fig.15, when interleaving L=15 bit input data, the interleaving pattern table C 700 which describes an L ($\leqq LA \times LB$) bit interleaving pattern is generated by using the interleaving pattern table A which has the LA=4 bit interleaving pattern and the interleaving pattern table B which has the LB=4 bit interleaving pattern (① in Fig.15). In the same way as shown in Fig.13, the method for generating the interleaving pattern table C 700 is

$$C[i] = A[i\%LA] + LA \times B[i/LA],$$

wherein LA = 4. The table A defines the pattern in the horizontal direction of the table C and the table B defines the pattern in the vertical direction.

[0105] The result is written to the table C in a horizontal direction. Since the table C has the 16 bit interleaving pattern, the 15 bit interleaving is performed by reading out the table C sequentially in the vertical direction and by discarding a number equal to or larger than 15 when the number is read. (② in Fig.15).

[0106] As shown in Fig.15, the 15 bit interleaving is available by skipping the number equal to or larger than 15. Also, the table C which includes the 15 bit interleaving pattern can be generated to perform the 15 bit interleaving by inhibiting data equal to or larger than 15 from being written when writing data to the table C. That is, as shown in Fig.15, in the case of generating the 15 ($<4\times4$) bit interleaving pattern table C with the table A storing the 4 bit interleaving pattern and the table B storing the 4 bit interleaving pattern, it is possible to generate the 15 bit interleaving pattern table C by not writing a number larger than 14 (=15-1).

[0107] According to the seventh embodiment, from one interleaving pattern table (in the case of A=B), or from two interleaving pattern tables, for example, an interleaving pattern table which has a larger interleaving length is generated. Thus, a pattern of a certain interleaving length can be represented by a plurality of patterns of a smaller interleaving length. Therefore, a memory amount for fixed length patterns can be decreased.

[0108] For example, conventionally, in the case of using a 1000 bit interleaving pattern table, memory for the 1000 bit interleaving pattern table is necessary. According to the seventh embodiment, by representing a 1000 bit interleaving pattern table with a 20 bit interleaving pattern table and a 50 bit interleaving pattern table, the memory can be decreased to an amount for 70 (=20 + 50) bits.

[0109] In addition, by representing a 900 bit interleaving pattern table with a 20 bit interleaving pattern table and a 50 bit interleaving pattern table, interleaving for 1000 bits and 900 bits is possible without enlarging the fixed length interleaving pattern table.

[0110] Next, an eighth embodiment will be described. According to the eighth embodiment of the present invention, the same result as that of the seventh embodiment shown in Fig.13 - Fig.15 is obtained. However, the interleaving pattern table C is not generated for interleaving, instead of that, an interleaving destination is directly obtained by calculating it from the table A and the table B. Fig.16 and Fig.17 show the eighth embodiment.

[0111] In Fig. 16, an example of a 16 bit input series in which the same result as that of Fig.13 can be obtained is shown.

[0112] As shown in Fig.16 , the interleaving pattern table C is not generated, unlike the example of Fig.13. Each destination for interchanging a bit in the input series is calculated (① in Fig.16) from the table A storing the 4 bit interleaving pattern and the table B storing the 4 bit interleaving pattern, thereby the input series is interleaved on the basis of the result of the calculation (② in Fig.16).

[0113] A formula for calculating directly the interleaving destination which is a jth element corresponding to an ith element in the input series from the table A and the table B is

$$C[i] = 4B[i\%4] + A[i/4]$$

[0114] The relationship between the table A and B can be interchanged. And, the interleaving pattern tables A and B can be the same or different patterns. If the table A and the table B are the same, it is necessary to use only one of the tables. That is,

$$j = 4A[i\%4] + A[i/4]$$
$$= 4B[i\%4] + B[i/4].$$

[0115] In Fig.17, interleaving pattern equations (710, 720) are used for defining interleaving instead of preparing for the interleaving pattern tables A and B. Also, interleaving is performed by calculating the interleaving pattern equation (①, ② in Fig.17).

[0116] The equation a 710 and the equation b 720 each of which equations represents a 4 bit interleaving pattern, are expressed as

$$ja = 2(ia\%2) + (ia/2) = fa(ia)$$

wherein $0 \leqq ia \leqq 4$

$$jb = 2(ib\%2) + (ib/2) = fb(ib)$$

wherein $0 \leqq ib \leqq 4$.

[0117] An interleaving destination which is a jth element corresponding to an ith element in the 16 bit input series is calculated by using both of the equation a and the equation b sequentially, which is the same as calculating

$$j = 4fa(i\%4) + fb(i/4)$$
$$= 8((i\%4)\%2) + 4((i\%4)/2) + 2((i/4)\%2) + ((i/4)/2),$$

thereby performing interleaving.

[0118] The relationship between the equation a and b can be interchanged. Also, the interleaving pattern equations a and b can be the same or different equations. If the equation A and the equation B are the same, it is necessary to use only one of the equations.

[0119] In the interleaving shown in Fig.17, it is also possible to perform interleaving after generating an interleaving pattern table by calculating a 16 bit interleaving pattern from the prepared 4 bit equations and writing the result of the calculation in the table, which is the same as the case of the seventh embodiment in which an interleaving pattern is defined by formulas instead of a pattern table.

[0120] According to the eighth embodiment, from one interleaving pattern table (when A = B), or from two interleaving pattern tables, interleaving of a larger interleaving length is performed. Therefore, it is characterized there is no need to generate another interleaving pattern table.

[0121] Further, from one interleaving pattern equation (when a = b), or from two interleaving pattern equations, interleaving of a larger interleaving length can be performed. In this case, it is unnecessary to generate another interleaving pattern table. However, it is possible to generate an interleaving pattern table.

[0122] A ninth embodiment will be described in the following. The ninth embodiment is an example in which a process shown in the seventh embodiment or the eighth embodiment is applied repeatedly a plurality of times. The ninth embodiment will be described with reference to Fig. 18 - Fig.22.

[0123] Fig. 18 shows an example in which a 16 bit interleaving pattern table is generated from two 2 bit interleaving pattern tables A, B and a 4 bit interleaving pattern table C by applying a process shown in the seventh embodiment in Fig. 13 repeatedly a plurality of times.

[0124] As shown in Fig. 18, when interleaving L=16 bit input data, an interleaving pattern table D 730 which has an L = 4(≦LA×LB) bit interleaving pattern is generated by using the interleaving pattern table A which has an LA=2 bit interleaving pattern and the interleaving pattern table B which has an LB=2 bit interleaving pattern (① in Fig. 18).

[0125] An operation for generating the interleaving pattern table D 730 is, for example,

$$D[i] = 2A[i\%2] + B[i/2],$$

(when the table A defines a writing direction of the table D and the table B defines a direction perpendicular to the writing direction of the table D.)

[0126] Next, an interleaving pattern table E 740 which has LE = 16(≦LC×LD) bit interleaving pattern is generated by referring to the generated interleaving pattern table D and the interleaving pattern table C which has an LD=4 bit interleaving pattern (② in Fig. 18).

[0127] An operation for generating the interleaving pattern table E 740 is, for example,

$$E[i] = 4D[i\%4] + C[i/2],$$

(in the case that the table D defines a horizontal direction of the table E and the table C defines a vertical direction of the table E.)

[0128] By referring to the interleaving pattern table E which was thus generated, interleaving of the 16 bit series is performed (③ in Fig. 18).

[0129] The relationship between the table A and B can be interchanged. Also, the interleaving pattern tables A and B can be the same or different patterns. If the tables A and B are the same, it is necessary to use only one of the tables can be used. That is,

$$C[i] = A[i\%4] + 4A[i/4]$$
$$= B[i\%4] + 4B[i/4].$$

In addition, the reading direction is not necessarily the same as the writing direction, and the both directions are not necessarily the same as shown in Fig. 18.

[0130] Fig. 19 shows an example in which 16 bit interleaving is performed with two 2 bit interleaving pattern tables A, B and a 4 bit interleaving pattern table C by assembling processes shown in the eighth embodiment in Fig. 16 repeatedly a plurality of times.

[0131] As shown in Fig. 19, the interchanging destination which is a jdth bit corresponding to an idth (0≦id<4) bit in a 4 bit series is calculated by referring to the table A and the table B. The operation is, for example,

$$jd = 2A[id\%2] + B[id/2]$$

in a case where the table A defines a writing direction of the table C and the table B defines a direction perpendicular to the writing direction of the table C.

[0132] Next, the interchanging destination which is a jth bit from a ith (0≦i<16) bit in a 16 bit input series 750 is calculated by referring to the result of the above mentioned operation and the interleaving pattern table C (② in Fig. 19). The operation is, for example,

$$j = 4 \times jd + C[i/4]$$

wherein jd is a interchanging destination of id=i%4.

[0133] Finally, interleaving is performed by interchanging the bit sequence of the 16 bit series on the basis of the result of the above mentioned operations (③ in Fig. 19).

[0134] The relationship between the table A and B can be interchanged. Also, the interleaving pattern tables A and B can be the same or different patterns. If the tables A and B are the same, it is necessary to use only one of the tables. In such a case,

$$C[i] = A[i\%4] + 4A[i/4]$$
$$= B[i\%4] + 4B[i/4]$$

can be applied.

[0135] Also, an interleaving pattern table can be generated by storing the result of the calculation in a table.

[0136] Fig.20 shows an example in which a process shown in Fig.17, which shows the eighth embodiment which defines interleaving by equations, is repeated.

[0137] As shown in Fig.20, first, an equation d for describing a 4 bit interleaving pattern, which is

$$jd = 2(id\%2) + (id/2),$$

is generated from an equation a (ja = ia) and an equation b (jb = ib), each of which equations describes a 2 bit interleaving pattern (① in Fig.20).

[0138] Next, a 16 bit interleaving equation e, which is

$$je = 8((ie\%4)\%2) + 4((ie\%/4)/2) + 2((ie/4)\%2) + ((ie/4)/2),$$

is calculated from the 4 bit equation c and the equation d (② in Fig.20). Then, interleaving is performed with the calculated equation e (③ in Fig.20).

[0139] It is also possible to perform interleaving after generating an interleaving pattern table by writing the result of the above mentioned calculation to a table.

[0140] Fig.21 shows an example in which interleaving is performed by defining an interleave with an equation and a table and generating an interleaving pattern table on the basis of the interleave.

[0141] As shown in Fig.21, a 4 bit interleaving equation d, which is

$$jd = 2(id\%2) + (id/2),$$

is generated from an equation a describing a 2 bit interleaving pattern and a 2 bit interleaving pattern table B (① in Fig.21).

[0142] Next, a 16 bit interleaving pattern table E 760 is generated by

$$E[i] = 4(2(i\%4)\%2) + ((i\%4)/2) + B[i/4]$$

from the equation d and a 4 bit interleaving pattern table C (② in Fig.21). Then, interleaving is performed with reference to the table E 760 (③ in Fig.21).

[0143] Fig.22 shows an example, which is a modification of Fig.13, in which example a 16 bit interleaving pattern table is generated from a plurality of 4 bit tables.

[0144] As shown in Fig.22, a 16 bit interleaving pattern table C 770 is generated by

$$C[i] = Ai/4[i\%4] + 4B[i/4]$$

(in the case that the table A0 - A3 defines the writing direction of the table C and the table B defines the perpendicular direction to the writing direction of the table C) with a plurality of 4 bit tables A0 - A3 and a 4 bit table B (① in Fig.22). Then, interleaving is performed by referring to the table C (② in Fig.22).

[0145] The relationship between the tables A0 - A3 and B can be interchanged. Also, the interleaving pattern tables A0 - A3 and B can be the same or different patterns. The reading direction is not necessarily downward and the writing direction is not necessarily rightward.

[0146] Next, an tenth embodiment will be described. The tenth embodiment shows a method in which interleaving is defined by an interleaving pattern description language, which is recognized so that an interleaving pattern is generated or interleaving is performed as was described in the above mentioned seventh - ninth embodiments.

[0147] Fig.23 - Fig.26 are figures for explaining the definition of the interleaving pattern description language. Fig.27 - Fig.31 shows examples in which a formula described by the interleaving pattern description language which is defined by Fig.23 - Fig.26 is recognized and an interleaving pattern is generated according to one of the methods or a combination of the methods shown in the above mentioned seventh - ninth embodiments so as to perform interleaving. Fig.32 is a diagram for explaining automatic generation of an interleaving pattern. Fig.33 shows a flowchart for explaining a flow of determining the interleaving pattern.

[0148] First, the interleaving pattern description language will be described with reference to Fig.23 - 26.

[0149] Fig.23 describes definition 1 of an interleaving pattern description language L [N×M]. L[N×M] means an N×M

block interleaver. This interleaver means performing interleaving of an L bit series with the NxM block interleaver. Fig.23 shows interleaving of the L bit series by the L[Nx M] block interleaver as an example.

[0150] Fig.24 describes a definition 2 of R{A}. R{A} means that A bits are rearranged in inverse order. Fig.24 shows R{6} as an example in which 6 bit series are rearranged in inverse order.

[0151] Fig.25 describes a definition 3 of L[N1x M1, N2xM2 • •]. L[N1xM1, N2xM2 • •] means interleaving of a plurality of series (each series is L bit length) by corresponding interleavers. Fig.25 shows 6[3x2, 2x3] as an example in which each of two 6 bit series is interleaved.

[0152] Fig.26 describes a definition 4 of L[N1[N2 xM2] xM1]. L[N1[N2xM2] xM1] means that after interleaving an L bit series by an N1xM1 block interleaver, each of M1 column arrays (N1 bits) is interleaved by an N2xM2 interleaver.

[0153] L[N1xM1 [N2xM2]] means that after interleaving an L bit series by an N1xM1 block interleaver, each of N1 row arrays (M1 bits) is interleaved by an N2xM2 interleaver.

[0154] Fig.26 shows 16[4[2x2]x4] as an example in which a 16 bit series 780 is written to a 4x4 block interleaver A 790 and each column array is read and interleaved by one of four 2x2 interleavers B - E. An interleaver F 800 is used for getting together the results by the interleavers B - E.

[0155] The above mentioned interleaving description language can be used for generating an interleaving pattern and performing interleaving of an input series by referring an interleaving pattern.

[0156] In the following, embodiments of interleaving by the above mentioned interleaving pattern description language will be described.

[0157] Fig.27 shows an example in which generation of an interleaving pattern described as 16[4[2x2]x4[2x2]] by the interleaving pattern description language is realized.

[0158] The meaning of the interleaving pattern described as 16[4[2x2]x4[2x2]] is as follows:

(a) First stage interleaver which is a 4x4 block interleaver performs 16 bit interleaving.
(b) Each of row arrays (4 bits) of the first stage interleaver is interleaved by a 2x2 interleaver.
(c) Each of the column arrays (4 bits) of the first stage interleaver is interleaved by a 2x2 interleaver.

[0159] Fig.27 describes how the above process is realized. As shown in Fig.27, an input 16 bit series 810 is written to a 4x4 block interleaver A 820 (① in Fig.27). Next, each of row data is read from the interleaver A 820 and interleaved by one of 2x2 interleavers B - E (② in Fig.27). The interleaved data is written to a interleaver F 830 (③ in Fig.27). Then, each of column data is read and interleaved by one 2x2 interleaver G - J (④ in Fig.27).

[0160] Finally, a described interleaving pattern is generated by writing the interleaved data to a table 840 (⑤ in Fig.27).

[0161] Fig.28 shows an example in which an interleaving process represented as 16[4[2x2]x4[2x 2]], which is the same description as shown in Fig.27, is realized by the above mentioned interleaving method. In Fig.28, the description of ① - ⑤ for generating an interleave patter will be omitted since it has been described with Fig.27. After that, interleaving can be realized by referring to the generated interleaving pattern table 850 (⑥ in Fig.28).

[0162] Fig.29 and Fig.30 shows examples in which a formula described by the above mentioned interleaving pattern description language is recognized and an interleaving pattern is generated according to one of the methods or a combination of the methods shown in the above mentioned seventh - ninth embodiments so as to perform interleaving.

[0163] Fig.29 shows that generation of an interleaving pattern or an interleaving process described as 16[4[2x2]x4[2x2]] is performed by applying interleaving processes shown, for example, in the above Fig.13 repeatedly.

[0164] In order to use an interleaving pattern described by the interleaving pattern description language according to Fig.29, first, interleaving pattern tables E and F are generated with interleaving pattern tables A - D (① and ②). Second, an interleaving pattern table G 860 is generated by calculating with the interleaving pattern tables E and F (③ in Fig.29). When interleaving is required, it is performed with the interleaving pattern table G 860 (④ in Fig.29).

[0165] Fig.30 shows that generation of an interleaving pattern or an interleaving process described as 16[4[2x2]x4[2x2]] is performed by applying interleaving processes shown, for example, in the above Fig.17 repeatedly.

[0166] As shown in Fig.30, 4 bit interleaving pattern equations e and f is generated from 2 bit interleaving pattern equations a - d (① and ② in Fig.30). Next, a 16 bit interleaving pattern equation g is generated from the 4 bit interleaving pattern equations e and f (③ and ④ in Fig.30) and interleaving is performed with the interleaving pattern equation g (⑤ in Fig.30).

[0167] After the generated interleaving pattern is stored, same interleaving process can be done only by reading the pattern table without generating the pattern once again at the time of next interleaving or other interleaving. Fig.31 shows as example of such an effect.

[0168] Fig.31 shows a case interleaving described as 16[4[2x2]x4[2x2]] is required assuming that a 4 bit interleaving pattern 4[2x2] is already stored.

[0169] For example, the case shown in Fig.31 takes the same method as that shown in Fig.29. As shown in Fig.31, a system has an interleaving pattern 4[2x2] as interleaving pattern tables A and B. Therefore, a 16 bit interleaving pattern

can be generated by referring to the 4 bit interleaving patterns (① in Fig.31) without performing a process corresponding to 4[2×2] (① and ② in Fig.29). Then interleaving is performed by referring to the generated interleaving pattern table C (② in Fig.31).

[0170] Thus, 16[4[2×2]×4[2×2]] can be generated from the stored 4[2×2] interleavers.

[0171] The method for realizing interleaving patterns described by interleaving pattern description languages shown in Fig.27 - Fig.31 is not limited to the methods shown here, for example, those methods can be combined. Therefore, for getting an interleaving pattern, either of an interleaving pattern table or an interleaving pattern equation can be used.

[0172] In the following, the generation method of the above mentioned interleaving pattern will be described by a flowchart shown in Fig.32.

[0173] As shown in Fig.32, when data of interleaving length L bits is given, first stage interleaving pattern N1×M1 which is equal to or larger than L bits is determined in step 102. Next, in step 104, a plurality of second stage interleaving patterns are determined each of which pattern corresponds to row array and column array of the first stage interleaver. Then, in step 106, interleaving patterns of third stage interleavers corresponds to each of the second stage interleavers in the same way as step 104. In step 108, the above process will be repeated until interleaving is not available anymore or until any stage, finally, in step 110, an interleaving pattern which can be described by an interleaving pattern description language is generated.

[0174] As the method for determining the interleaving pattern of the interleaver of each stage, methods of using factoring, referring to a list, and using a real number near the result of squaring the interleaving length of each stage, and selecting an odd number or a prime number for N or M in the N× M interleaver of each stage in the above each methods can be used.

[0175] The above mentioned method will be called a multi stage interleaving method.

[0176] Fig.33 is a flowchart for selecting a feasible interleaving pattern among the generated interleaving patterns.

[0177] As shown in Fig.33, an interleaving pattern corresponding to an interleaving length is generated in step 204 as described with Fig.32, and the generated interleaving pattern is tested in step 206.

[0178] If the test is unsuccessful, all or a part of the patterns of each stage interleaver shown in Fig.32 are changed and the interleaving pattern is regenerated in step 204. The above process will be repeated until the test becomes successful in order to determine an eventually generated interleaving pattern.

[0179] Items of the test may be intensity of resistance to burst error, intensity of randomness of interleaved bits, and the like. In particular, if the interleaver is assumed to be used as a turbo code interleaver, a code weight test, a code weight test assuming trellis termination and the like may be used for the test.

[0180] According to the above description, it is obvious that the methods of the present invention can be applied to any interleaving unit such as a symbol other than a bit. Further, the length of interleaved series may change over time.

[0181] According to the method for generating an interleaving pattern of the present invention described in the seventh - tenth embodiment, memory capacity can be reduced and an interleaving length without a corresponding interleaving pattern can be processed flexibly. That is, when interleaving 1000 bit series without using the method of the present invention, a table which includes interleaving pattern for the 1000 bits is necessary. Therefore, the longer the interleaving length, the more the memory amount for storing an interleaving pattern table, in which the interleaving length means the total number of interleaved units such as bits, symbol, and the like. Further, without the present invention, when the interleaving length changes, sufficient interleaving patterns need to be prepared such that each interleaving pattern corresponds to a changed interleaving length. Thus, the more the kinds of the interleaving length, the more the memory amount for storing the interleaving pattern tables corresponding to each interleaving length. For example, for 4 kinds of interleavers of 10 bits, 100 bits, 1000 bits, 10000 bits interleaving length, memory amount for

$$10([\log(10-1)]+1)+100([\log(100-1)]+1)+1000([\log(1000-1)]+1)+10000([\log(10000-1)]+1)$$

bits is necessary in order to store the every interleaving patterns, in which [log X] means that the logarithm X to the base 2 is taken and the fractional portion of the number is dropped, therefore, [log (X-1)]+1 means the number of digits of the integer X in binary notation. According to the present invention, such a problem will nor arise. Further, according to the present invention, an interleaving pattern can be generated as a description by an interleaving pattern description language. The characteristics of the generated interleaving pattern can be checked, and, it is possible to add a system in which an interleaving pattern of good characteristics is regenerated automatically if the checked characteristics is bad.

[0182] Next, embodiments of the present invention for achieving the third objectives will be described. In the following, an interleaving method for a turbo encoder, a transmission system of a transmitter-receiver in mobile communication and the like will be described. Before describing the embodiments, the configurations of the turbo encoder and the transmitter-receiver in mobile communication will be described.

[0183] Fig.34 (a) is a diagram showing a configuration of the turbo encoder. The turbo encoder is formed by including recursive systematic convolutional encoders (RSC 12, RSC 13), in which the recursive systematic convolutional encoder is shown in Fig.34 (b). As shown in Fig.34 (a), input data d is processed and output as output data X1 - X3. An

interleaver 11 is placed before the recursive systematic convolutional encoder (RSC) 13 in order to reduce interrelationship between the redundant bits X1 and X2. In addition, a turbo decoder includes 2 decoders, an interleaver and a deinterleaver which performs a reverse process of an interleaver.

[0184] Fig.35 is a diagram showing a part of the configuration of a transmitter-receiver and the like of CDMA in mobile communication. In the transmitting end, after a channel encoder 21 performs channel encode, a channel interleaver 22 performs interleaving. Then, SS transmitter 23 time-division multiplexes modulated signals and pilot symbols, and performs spread modulation. In the receiving end, a RAKE receiver 25 performs despreading, and, then, performs RAKE synthesis by using pilot symbols. A channel deinterleaver 26 performs deinterleaving and a channel decoder 27 performs decoding. If the turbo code is used for a transmission system, a turbo encoder instead of the channel encoder 21 is used, and a turbo decoder instead of a channel decoder 27 is used.

[0185] The table of the interleaver used in these devices is, for example, one described in Fig.12.

[0186] In the following, examples of deinterleaving which is performed in the channel deinterleaver 26 and the like are described with reference to Fig.36 and Fig.37.

[0187] Fig.36 (a) shows an example in which interleaving of 12 bits is performed with a table A (LA=3 bits) and a table B. The operation for generating an interleaving pattern table C[i] (ith bit of bit sequence C) is

$$C[i] = LB \times A[i\%LA] + B[i/LA]$$

in which LA = 3 and LB = 4. In addition, the table A defines the pattern in a vertical direction of the table C and the table B defines the pattern in a horizontal direction of the table C. By calculating the operation, an interleaving pattern table C is generated, and an output data is obtained from an input data by referring to the interleaving pattern table C.

[0188] Fig.36 (b) shows a deinterleaving process which is a reverse process to the above mentioned process. A deinterleaving pattern table C 870 can be generated by interchanging the table A and the table B and by performing the same operation. If input data is 0, 8, 4, 2, • • •, 7 which is the output of the above mentioned interleaving, the output becomes 0, 1, 2, • • •, 11 which is the input of the above mentioned interleaving.

[0189] Fig.37 (a) shows an example of interleaving in the case of LA×LB>L, and Fig.37 (b) shows deinterleaving. In Fig.37 (a), a value which is equal to or larger than L is not read out, or, the value is not written when generating a table. The operation formula in Fig.37 (c) is

$$C[i] = LB \times A[i\%LA] + B[i/LA] -$$

in which follows the following rule (represented by C language).

```
=0
for(j=0,J<(LA×LB-L),J++){
if C[i]>=LB×A[(L-1-j)%LA]
                +B[(L-1-j)/LA]
    ++;
}
```

[0190] The deinterleaving method can be applied to the above mentioned interleaving methods and also applied to the after-mentioned interleaving methods.

[0191] Next, an eleventh embodiment will be described. In the following description, notation for describing an interleaving pattern is the one used in Fig.23 - Fig.25.

[0192] In the following, a generating method of an interleaving pattern suitable for turbo code with reference to Fig.38 - Fig.45.

[0193] Fig.38 is a flowchart for explaining a generating method of an interleaving pattern which has an L bit interleaving length and is suitable for turbo code.

[0194] From the first stage (S302) to the higher stage (S306) shown in Fig.38, the interleaving pattern for turbo code having L bit interleaving length is determined by a decision process which will be described in detail with Fig.39. Interleave patterns are determined when all processes of each decision process branch are completed, and, then, the interleaving pattern is generated from the determined final results (S308). After that, the generated interleaving pattern are checked and the interleaving pattern of the L bit interleaving length which is suitable for turbo code can be obtained.

[0195] Now, the decision process of the interleaving pattern will be described. Fig.39 is a diagram showing the deci-

sion process of the interleaving pattern in detail. Fig.40 is a table showing a list of predefined interleaving patterns (PIP) which are used for the decision process of the interleaving pattern. The predefined interleaving pattern list is a list of interleaving patterns which is recognized to be suitable for turbo code.

[0196] In the first stage (S302) in Fig.38, it is necessary to determine an interleaving pattern represented by row and column of $L \leq N^1 \times M^1$ (the superscript denotes the number of the stage). In this eleventh embodiment, N^1 is fixed to be 7. Thus, M^1 is determined such that if a value of L divided by 7 is an integer, M^1 is the value, and, in the other cases, M^1 is a minimum integer larger than the value. The predefined interleaving pattern corresponding to N^1 is R{7[3x3[2x2]]} which is shown in Fig.40 as T7.

[0197] It is necessary to represent each of 7 rows (M_1^1 - M_7^1) as a row and a column in order to determine the row and the column of the interleaving pattern of the first stage. Thus, in the second stage, a row and a column need to be determined in each of 7 branches corresponding to each of the rows (refer to Fig.39). In order to determine the row and the column, as shown in the second stage (S304) in Fig.38, the number of each of columns M_Y^2 (Y=1, 2, • •, 7) is selected from "7, 13, 17, 29, 37, 43, 59 (L>3000 bits)" or "5, 7, 11, 13, 17, 37, 43 (3000>L≧301 bits)" which are shown in PIP lists in Fig38. The number of the row N_Y^2 is determined such that if a value of M^1 divided by the selected number of M_Y^2 is an integer, N_Y^2 is the value, and, in the other cases, N_Y^2 is a minimum integer larger than the value. If an IP (interleaving pattern) corresponding to the N_Y^2 is defined in the table in Fig.40, the operation to the branch is completed. If not, the process moves to the next stage (S306).

[0198] In the next process (S306), the process to determine a row and a column until the undetermined rows are determined. In the process (S306), each branch is processed as described below and as shown in Fig.39. The number of a column M_Y^Z (Z≧3) is defined to be a number which is equal to or smaller than the square root of the undefined number of row $N_Y^{(Z-1)}$ of previous stage and is a maximum number in PIP (except for 4 and 6) in Fig.40. The reason for excluding 4 and 6 is that it is known empirically that an odd number or a large number is suitable for the column number for turbo code. The number of the row N_Y^Z is determined such that if a value of $N_Y^{(Z-1)}$ divided by the above defined M_Y^Z is an integer, N_Y^Z is the value, and, in the other cases, N_Y^Z is a minimum integer larger than the value. If PIP is defined for the row number N_Y^Z in Fig.40, the process of the branch is completed. The process will be performed until every branch of every stage is completed.

[0199] In addition, other than interleaving patterns shown in Fig.40, an interleaving pattern corresponding to other number can be defined. In this case, the interleaving pattern corresponding to the other number is generated by the same method as that in higher stage shown in Fig.38. The more the interleaving patterns defined in Fig.40, the fast a process is completed. Even when the number of the interleaving patterns shown in Fig.40 is increased in such away, M_Y^Z (Z≧3) will be selected among "2, 3, 5, 7, 8, 9, 11, 13, 17, 20, 29, 37, 43, 47, 53, 59, 61" shown in Fig.40.

[0200] . After all interleaving patterns of the row and the column are defined, the interleaving pattern is generated from the defined interleavers of the row and the column (S308). The process will be described with reference to Fig.41 - Fig.44 in detail.

[0201] Fig.41 is a diagram showing a detailed generating process of the interleaving pattern by the above mentioned multistage interleaving method. As is understood from this figure, the interleaving pattern (IP) corresponding to the row or the column of the upper stage is determined from the interleaving pattern (IP) corresponding to the row or the column defined in the lower stage, which is reverse of the procedure of each branch in Fig.39. Then, the L bit interleaving pattern (IP) can be generated finally.

[0202] The way in which the interleaving pattern (IP) is generated by the interleaving patterns of the row and the column will be described in detail with reference to Fig.42 - Fig.44. Fig.42 is a diagram for explaining one stage of the generating process of the interleaving pattern. Fig.43 is an example of the generating process shown in Fig.42. Fig.44 is a diagram for explaining the final stage of the generating process of the interleaving pattern.

[0203] Fig.42 shows how the interleaving pattern of N_Y^Z (= $N_Y^{(Z+1)} \times M_Y^{(Z+1)}$) bits of each branch is generated by using an $N_Y^{(Z+1)}$ bit interleaving pattern (IP) corresponding to the column which is determined in the lower stage and an $M_Y^{(Z+1)}$ bit interleaving pattern corresponding to the row which is determined in the lower stage.

[0204] In Fig.42, by the operation to the $N_Y^{(Z+1)}$ bit interleaving pattern (IP) corresponding to the column and the $M_Y^{(Z+1)}$ bit interleaving pattern (IP) corresponding to the low, a pattern C'[i] of N_Y^Z bits is generated in each branch. The C'[i] represents an ith element of the pattern C'. The operation is

$$C'[i] = M_Y^{(Z+1)} A[i \% N_Y^{(Z+1)}] + B[i / N_Y^{(Z+1)}],$$

wherein A represents an interleaving pattern corresponding to $N_Y^{(Z+1)}$ of the column, B represents an interleaving pattern corresponding to $M_Y^{(Z-1)}$ of the row, "%" is a modulo operator which takes a remainder of division, and "/" means an integer part (in which fractional portion is dropped) of division.

[0205] The pattern C' by the operation is written to a memory which has a capacity of vertical $N_Y^{(Z+1)}$ x horizontal $M_Y^{(Z+1)}$ in a vertical direction. Then, N_Y^Z bit interleaving pattern C is obtained by reading out the memory in a vertical direction. At the time, the interleaving pattern C can be obtained without writing a number which is equal to or larger

than N_Y^Z to the memory when N_Y^Z is smaller than $N_Y^{(Z+1)} \times M_Y^{(Z+1)}$. Also, the interleaving pattern can be obtained by writing all data in the memory and skipping a number larger than N_Y^Z when reading.

[0206] Fig.43 shows a concrete example of the process. Fig.43 shows an example in which a 15 bit interleaving pattern (IP) C which is smaller than 4 x 4 =16 is obtained from a 4 bit interleaving pattern (IP) A and a 4 bit interleaving pattern (IP) B.

[0207] As shown in Fig.43, an 16 bit interleaving pattern C' is obtained by an operation with a 4 bit interleaving pattern A = {0, 2, 1, 3} and a 4 bit interleaving pattern B = {0, 2, 1, 3}. Then, the pattern is written to a 4 x 4 memory sequentially in a vertical direction. The operation is

$$C'[i] = 4A[i\%4]+B[i/4].$$

At this time, "15" obtained by the operation is not written to the memory. A 15 bit interleaving pattern C can be obtained by reading out data from the memory in the same direction as writing sequentially.

[0208] Thus, interleaving patterns (IP) corresponding to each row and each column from the final stage to the second stage, and, then, interleaving patterns corresponding to the first row - the seventh row of the first stage can be obtained. Finally, the L bit interleaving pattern is obtained from the interleaving patterns of the first row - the seventh row.

[0209] Fig.44 is a diagram for explaining how the L bit interleaving pattern is generated from a plurality of rows in the first stage. As shown in Fig.44, the L bit pattern C is generated from an N bit interleaving pattern (IP) corresponding to the column and N interleaving patterns corresponding to each row.

[0210] In Fig.44, assuming that N which is the column as A, and assuming each of M_0 - $M_{(n-1)}$ which is the row as B_0 - $B_{(n-1)}$, the operation is represented as

$$C[i] = MA[i\%] + B_{i\%N}\,[i/N]$$

Which is different from that in Fig.43 and B is changed. The L bit interleaving pattern C can be generated by writing to a memory sequentially in a vertical direction and reading out sequentially in a vertical direction. The process when L<MxN is the same as that described in Fig.43.

[0211] As mentioned above, the L bit length interleaving pattern can be generated (S308 in Fig.38). In Fig.38, the generated interleaving pattern is checked next (S310). If the generated interleaving pattern is rejected according to the check, an interleaving pattern is regenerated by changing N to 7 represented by R(7[3×R{3}])), and a better interleaving pattern is selected by comparing the regenerated pattern with the former interleaving pattern.

[0212] The checking method of the generated interleaving pattern will be described with reference to Fig.45. As shown in Fig.45, interleaved L bit series is compared with L bit series which is not interleaved, and, if all bits or a part of bits within 30 bits from the last bit of the bit series which is not interleaved are interleaved within 30 bits from the last bit of the interleaved bit series, the interleaving pattern which performs the interleaving is rejected.

[0213] The interleaving pattern obtained by the flowchart shown in Fig.38 is suitable for turbo coding. The turbo code is assumed to be turbo code of constraint length 3. That is, it means there are two delay elements D such as (16) and (17) (constraint length - 1). When assuming turbo code of constraint length 4 , N^1 of the first stage in Fig.38 can be set as 8 represented by R{8[4[2x2]x 2]}. That is, M^1 becomes L/8 and the number of the branches shown in Fig.41 increases to 8 from 7.

[0214] Next, a twelfth embodiment will be described.

[0215] In the following, a generating method of an interleaving pattern suitable for transmission line interleaver with reference to Fig.46 - Fig.49.

[0216] Fig.46 is a flowchart for explaining a generating method of an interleaving pattern which is suitable for transmission system.

[0217] From the first stage (S402) to the higher stage (S406) shown in Fig.46, the interleaving pattern for transmission line interleaver having L bit interleaving length is determined by a decision process which will be described in detail with Fig.47. Interleave patterns are determined when all processes of each decision process branch are completed, and, then, the interleaving pattern is generated from the determined final results (S408).

[0218] Now, the decision process of the interleaving pattern will be described. Fig.47 is a diagram showing the decision process of the interleaving pattern in detail. Fig.48 is a table showing a list of predefined interleaving pattern (PIP) which is used for the decision process of the interleaving pattern. The predefined interleaving pattern list in Fig.48 is a list of interleaving patterns which are recognized to be suitable for transmission system.

[0219] In the first stage (S402) in Fig.46, it is necessary to determine an interleaving pattern represented by a row and a column of $L \leqq N^1 \times M^1$ (the superscript denotes the number of the stage). M^1 which is the number of the column in the first stage is selected among 16, 32, 64, 128 according to the number of slots (interleaving length) in one frame. N^1 which is the number of row in the first stage is determined as a minimum integer larger than L divided by the selected M^1.

[0220] In the second stage (S404), M^2 is selected among numbers corresponding to the list of the predefined interleaving patterns shown in Fig.48 (excluding "13" and "17") as a number which can divide N^1 and is a maximum integer which is equal to or smaller than the square root of N^1. If the integer is smaller than $\sqrt{N^1}/4$ (the square root of N^1 /4) or if there is no divisible candidate in the PIP list, a maximum integer which is equal to or smaller than the square root of N^1 is selected in the PIP list (excluding "13" and "17"). The reason for excluding 13 and 17 is that it is known empirically that an even number is suitable for transmission system. N^2 is a minimum integer which is equal to or larger than N^1 divided by the selected M^2. In the second stage (S404), if N^2 is defined in the PIP list in Fig.48, all interleaving patterns are determined, thereby the process of generating the L bit interleaving pattern is performed with the determined interleaving pattern (S408). If N^2 is not defined in the PIP list, the process moves to the next stage (S406). (refer to Fig.47)

[0221] In the stage (S406), similar to the second stage, M^Z ("Z" represents the number of stage) is selected among numbers corresponding to the predefined interleaving patterns shown in Fig.48 (excluding "13" and "17") as a number which can divide N^1 and is a maximum integer which is equal to or smaller than the square root of N^1. If the integer is smaller than $\sqrt{N^1}/4$ (the square root of N^1 /4) or if there is no divisible candidate in the PIP list, a maximum integer which is equal to or smaller than the square root of N^1 is selected in the PIP list (excluding "13" and "17"). N^Z is a minimum number which is equal to or larger than previous stage $N^{(Z-1)}$ divided by the selected M^Z. Such a process is performed until N^Z is defined in PIP in Fig.48 (refer to Fig.47). If it is defined, since all interleaving patterns are defined, the process for generating the L bit interleaving pattern is performed with the determined interleaving patterns (S408).

[0222] In addition, other than interleaving patterns shown in Fig.48, an interleaving pattern corresponding to other number can be defined. In this case, the interleaving pattern corresponding to the other number is generated by the same way as that in higher stage shown in Fig.46. The more the interleaving patterns defined in Fig.48, the fast the process is completed. Even when the number of the interleaving patterns shown in Fig.48 is increased, M_Y^Z ($Z \geq 2$) will be selected among "2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 16, 20, 32, 64, 128" shown in Fig.48.

[0223] The process for generating the L bit interleaving pattern (S408) will be described with reference to Fig.49 showing a detailed generating process of the interleaving pattern by the above mentioned multistage interleaving method.

[0224] In Fig.49, by using interleaving patterns (IP) N^Z and M^Z, $N^{(Z-1)}$ of the former stage will be obtained. The obtaining process was described in Fig.42 and Fig.43, therefore, the description will be omitted. By performing the process sequentially, the L bit interleaving pattern which is suitable for transmission system can be obtained. In the above descriptions, bit length is used from interleaving pattern length. Different representations will be used as a unit other than bit for interleaving.

[0225] In the following, an interleaving device which uses the above mentioned interleaving method will be described as a thirteenth embodiment.

[0226] The interleaving method described so far can be applied to an interleaver and a deinterleaver in devices shown in Fig.34 - Fig.35. However, it is not limited to the devices. The multiple interleaving method of the present invention can be applied to other devices which perform interleaving. The present invention of the eleventh and twelfth embodiments is especially suitable for devices shown in Fig.34 - Fig.35, that is, a turbo encoder and a transmission system device.

[0227] Since the configurations of an interleaver and a deinterleaver are the same, an example of the interleaver will be described. Fig.50 shows an example of a device for performing interleaving or deinterleaving. As shown in Fig.50, the interleaver includes an input buffer 30, an output buffer 32, a memory 34, and a CPU 36. Input series data is stored in the input buffer and interleaved output series data is stored in the output buffer. In the case of deinterleaving, interleaved data is stored in the input buffer 30 and deinterleaved data which is the data before interleaving. The input buffer and the output buffer 32 are realized with a RAM, a shift register, and the like. The memory 34 stores the above mentioned interleaved pattern tables and/or a program which directly calculates interleaved addresses in the output buffer 32, and is realized by a RAM, a ROM and the like. The CPU 36 performs instruction of input/output to the buffers, address calculation, and so on. The above mentioned configuration can be realized by an integrated circuit such as an LSI and the like.

[0228] Next, the operation in the case that the memory 34 stores only interleaving pattern tables will be described.

[0229] When input series data is input in the input buffer 30, the CPU 36 reads out destination addresses in the output buffer with reference to an interleaves pattern table in the memory 34 and outputs the input series data to the addresses in the output buffer 32.

[0230] When calculating the addresses directly, the CPU 36 calculates the destination addresses by a program from addresses of the input series data in the input buffer 30 and outputs to the addresses in the output buffer 32.

[0231] In the following, a media according to the present invention will be described as a fourteenth embodiment. An interleaving pattern can be generated automatically and can be used as pattern data in the above mentioned RAM and the like by performing the interleaving pattern generating method, on a computer, which was described with flowcharts shown in Fig.38 and Fig.46 and is suitable for transmission system and turbo code.

[0232] At the time, interleaving patterns defined in Fig.40 and Fig.48 can be stored in a storage device and referred to by a program. Also, only representations may be stored and interleaving pattern may be generated if necessary. Fur-

ther, for example, common processes shown in Fig.39, Fig.41, and Fig.47, Fig.49 can be used as subroutines and used by calling from other processes.

[0233] The medium storing a program of the present invention can be realized by an electronic memory, a hard disk, a magneto-optical disk, a floppy disk and the like. the methods of the present invention can be performed and the interleaving pattern can be obtained by loading the program stored in the medium in a computer or incorporating the medium in a computer. Further, an encoder/decoder and a transmitter-receiver can be formed so as to generate an optimal interleaving pattern automatically by loading the program in a memory in the encoder/decoder and transmitter-receiver or incorporating the medium in the devices. Therefore, the devices can perform optimal interleaving processes under various conditions in communication.

[0234] As described above, by using the interleaving pattern generating method of the present invention, an interleaving pattern suitable for using purpose.

[0235] The present invention is not limited to the specifically disclosed embodiments, and variations and modifications may be made without departing from the scope of the invention.

Claims

1. An interleaving method for inputting a data series of a unit length and outputting an interleaved data series of the unit length, characterized by:

   a first step of writing data of said data series to a first interleaver, reading out the data column by column or row by row from said first interleaver, and writing the data to a plurality of second interleavers;
   a second step of reading out the data from each of said second interleavers, and writing the data to one or a plurality of third interleavers as necessary, and
   reading out the data from each of interleavers generated by repeating said second step once or a plurality of times, or from each of interleavers generated by said first step, and outputting said interleaved data series.

2. An interleaving method for inputting a data series of a unit length and outputting an interleaved data series of the unit length, characterized by:

   a first step of writing said data series to a first interleaver in one direction;
   a second step of reading out column data or row data from said first interleaver, writing said read out data to a second interleaver, which has a size different from a size of said first interleaver, in one direction, and repeating said reading out column data or row data and said writing read out data column by column or row by row;
   repeating a third step of performing said second step wherein each of a plurality of said second interleavers generated by said second step is regarded as said first interleaver, and
   reading out data from each of interleavers generated by repeating said third step or by performing said second step, and outputting said interleaved data series.

3. An interleaving method for inputting a data series of a unit length and outputting an interleaved data series of the unit length, characterized by:

   a first step of writing said data series to a first interleaver in one direction;
   a second step of reading out column data or row data from said first interleaver, writing said read out data to a second interleaver, which has a size different from a size of said first interleaver, in one direction, and repeating said reading out column data or row data and said writing read out data column by column or row by row;
   a third step of reading out data column by column or row by row from each of interleavers generated by said second step, and writing said data to an interleaver which has a size the same as the size of said first interleaver, and
   reading out data from said interleaver generated by said third step, and outputting said interleaved data series.

4. The interleaving method as claimed in claim 3, characterized by:

   a fourth step of performing said second step and said third step wherein said interleaver generated by said third step is regarded as said first interleaver, reading out data from an interleaver generated by repeating said fourth step once or a plurality of times, and outputting said interleaved data series.

5. An interleaving method for inputting a data series of a unit length and outputting an interleaved data series of the unit length, characterized by:

storing a plurality of interleaving patterns in a table beforehand;

applying one of said interleaving patterns to said input data series by referring to said table and outputting data, and

repeating a step of applying one of said interleaving patterns to said output data, and outputting said interleaved data series.

6. The interleaving method as claimed in claim 5, characterized in that an interleaving pattern is stored in said table according to said interleaving method as claimed in any one of claims 1 - 4.

7. A method for generating an interleaving pattern description of an interleaving pattern for interleaving an input data series of a unit length and outputting an interleaved data series of the unit length, characterized by:

generating said interleaving pattern description of a third unit by using an interleaving pattern description of a first unit and an interleaving pattern description of a second unit.

8. The method for generating an interleaving pattern description, characterized by generating said interleaving pattern description of a predetermined length unit by using said method for generating an interleaving pattern description as claimed in claim 7 for a plurality of times.

9. The method as claimed in claim 7 or 8, characterized in that said interleaving pattern description is an interleaving pattern table or an interleaving pattern equation which describes an interleaving pattern.

10. An interleaving method for inputting a data series of a unit length and outputting an interleaved data series of the unit length, characterized by:

generating an interleaving pattern description of a third unit by using an interleaving pattern description of a first unit and an interleaving pattern description of a second unit, and
interleaving with said generated interleaving pattern description.

11. An interleaving method for inputting a data series of a unit length and outputting an interleaved data series of the unit length, characterized by:

calculating interleaving destinations in a series of a third unit with an interleaving pattern description of a first unit and an interleaving pattern description of a second unit, and
interleaving with the result of the calculation.

12. An interleaving method characterized by:

generating an interleaving pattern description of a first unit and an interleaving pattern description of a second unit by using the interleaving pattern description generated by said method as claimed in claim 7 or 8,
interleaving a data series of a third unit by calculating from said interleaving pattern description of a first unit and said interleaving pattern description of a second unit.

13. The interleaving method as claimed in any one of claims 10 - 12, characterized in that said interleaving pattern description is an interleaving pattern table or an interleaving pattern equation which describes an interleaving pattern.

14. A method for generating an interleaving pattern description of an interleaving pattern for interleaving an input data series of a unit length and outputting an interleaved data series of the unit length, characterized by:

interpreting an interleaving pattern description language which defines an interleaving pattern, and
generating an interleaving pattern description by using said method as claimed in claim 9 on the basis of said interpretation.

15. The method as claimed in claim 14, characterized in that if an interleaving pattern description corresponding to a part of said interleaving pattern description language is stored, said interleaving pattern description is generated with reference to said stored interleaving pattern description without performing a process corresponding to said part of said interleaving pattern description language, when generating an interleaving pattern.

16. The interleaving method characterized by:

interpreting an interleaving pattern description language which defines an interleaving pattern, and interleaving by said interleaving method as claimed in claim 13 on the basis of said interpretation.

17. The interleaving method as claimed in claim 16, characterized in that if an interleaving pattern description corresponding to a part of said interleaving pattern description language is stored, said interleaving pattern description is generated with reference to said stored interleaving pattern without performing a process corresponding to said part of said interleaving pattern description language, when interleaving.

18. A method for generating an interleaving pattern description of an interleaving pattern for interleaving an input data series of a unit length and outputting an interleaved data series of the unit length, characterized by:

determining an interleaving pattern description of a first stage when a unit length is given, and
generating an interleaving pattern description by repeating a process of determining interleaving patterns corresponding to interleavers of a column and a row of a stage after said first stage until reaching any stage or until becoming unable to interleave.

19. A method for generating an interleaving pattern description of an interleaving pattern for interleaving an input data series of a unit length and outputting an interleaved data series of the unit length, characterized by:

checking an interleaving pattern description which is generated;
generating an interleaving pattern description again after changing all or a part of parameters if the result of said checking is unsuccessful, and
repeating said checking and said generation until the result of said checking becomes successful so as to generate an interleaving pattern description which passed said checking.

20. The method as claimed in claim 18 or 19, characterized in that said interleaving pattern description which is generated is an interleaving pattern table or an interleaving pattern equation or an interleaving pattern description language.

21. A method for generating an interleaving pattern description of an interleaving pattern for interleaving an input data series of a unit length and outputting an interleaved data series of the unit length, characterized by:

a step of determining, when a unit length is given, the number of rows or columns of a block interleaver corresponding to said unit length by using an interleaving pattern list suitable for a predefined application target and defining the number of columns or rows from said determined number of rows or columns, and
generating an interleaving pattern of said unit length from interleaving patterns obtained by repeating said step until said defined number of columns or said defined number of rows is defined in said interleaving pattern list.

22. The method as claimed in claim 21, characterized by:

a first step, which is a process of a first stage, of determining the number of rows or the number of columns of a block interleaver corresponding to a unit length which is given beforehand by a defined number, assuming an interleaving pattern corresponding said defined number as a predefined interleaving pattern, and defining the number of rows by using said determined number of columns or defining the number of columns by using said determined number of rows;
a second step of determining the number of rows or the number of columns of a block interleaver corresponding to said defined number of rows or said defined number of columns by using an interleaving pattern list suitable for a predefined application target, and defining the number of columns from said determined number of rows or defining the number of rows from said determined number of columns;
a third step of repeating said second step until an interleaving pattern corresponding to the number of rows or columns exists in said predefined interleaving pattern list;
performing said third step a number of times equal to the number of rows or columns corresponding to said predefined interleaving pattern in said first step, and
generating an interleaving pattern corresponding to the row or the column of a former stage sequentially from an interleaving pattern corresponding to the row and the column which is generated in a final stage.

23. The method as claimed in claim 21 or 22, further characterized in that said generated interleaving pattern of said unit length is checked and an interleaving pattern of said unit length is generated again according to the result of said checking.

24. The method as claimed in claim 22 or 23, characterize in that said application target is turbo code and the number of rows of said first stage is 7.

25. The method as claimed in claim 22 or 23, characterize in that said application target is transmission and the number of columns of said first stage is the number of slots of one frame.

26. An interleaving device for inputting a data series of a unit length and outputting interleaved data series of the unit length, characterized by:

means which stores one or a plurality of interleaving patterns in a table beforehand;
means which outputs data by applying one of said plurality of interleaving patterns, and
means which outputs said output data by further applying one of said plurality of interleaving patterns as necessary.

27. The interleaving device as claimed in claim 26, characterized in that said table stores an interleaving pattern by said interleaving method as claimed in one of claims 1 - 4.

28. The interleaving device as claimed in claim 26, characterized in that said interleaving pattern is generated by said interleaving pattern generating method as claimed in claim 21.

29. The interleaving device as claimed in one of claims 26 - 28, characterized in that interleaving destinations of an input data series are calculated, and the interleaving is performed on the basis of said calculation and data is output instead of using an interleaving pattern.

30. A computer readable medium storing a program for description and generation of an interleaving pattern in an interleaving method for inputting a data series of a unit length and outputting an interleaved series of the unit length, said program characterized by:

a step of determining the number of rows or columns of a block interleaver corresponding to a unit length which is given beforehand by using an interleaving pattern list suitable for a predefined application target and defining the number of columns from said determined number of rows or the number of rows from said determined number of columns, and
generating an interleaving pattern of said unit length from interleaving patterns obtained by repeating said step until said defined number of columns or said defined number of row is defined in said interleaving pattern list.

31. The computer readable medium storing a program for generation of an interleaving pattern as claimed in claim 30, said program characterized by:

a first step, which is a process of a first stage, of determining the number of rows or the number of columns of a block interleaver corresponding to a unit length which is given beforehand by a defined number, assuming an interleaving pattern corresponding said defined number as a predefined interleaving pattern, and defining the number of rows by using said determined number of columns or defining the number of columns by using said determined number of rows;
a second step of determining the number of rows or the number of columns of a block interleaver corresponding to said defined number of rows or said defined number of columns by using an interleaving pattern list suitable for a predefined application target, and defining the number of columns from said determined number of rows or defining the number of rows from said determined number of columns;
a third step of repeating said second step until an interleaving pattern corresponding to the number of rows or columns exists in said predefined interleaving pattern list;
performing said third step a number of times equal to the number of rows or columns corresponding to said predefined interleaving pattern in said first step, and
generating an interleaving pattern corresponding to the row or the column of a former stage sequentially from an interleaving pattern corresponding to the row and the column which is generated in a final stage.

32. The computer readable medium storing a program for generation of an interleaving pattern as claimed in claim 30 or 31, said program further characterized in that said generated interleaving pattern of said unit length is checked and an interleaving pattern of said unit length is generated again according to the result of said checking.

33. The computer readable medium storing a program for generation of an interleaving pattern as claimed in claim 31, characterize in that said application target is turbo code and the number of rows of said first stage is 7.

34. The computer readable medium storing a program for generation of an interleaving pattern as claimed in claim 31, characterize in that said application target is transmission and the number of columns of said first stage is the number of slots of one frame.

FIG. 1

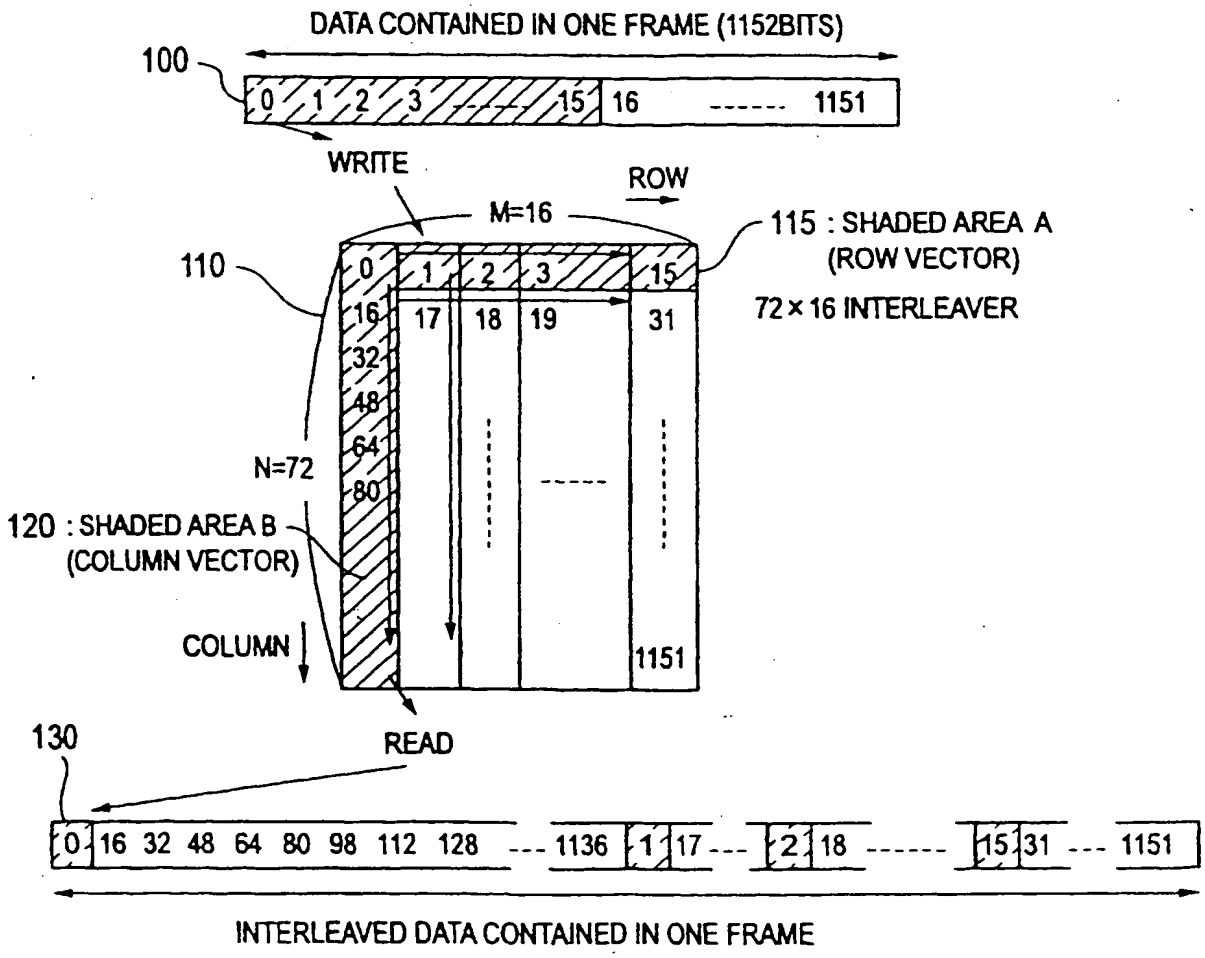

DATA CONTAINED IN ONE FRAME (1152BITS)
100
0 1 2 3 15 16 ------ 1151
WRITE
ROW
M=16
115 : SHADED AREA A
(ROW VECTOR)
72 × 16 INTERLEAVER
110
0 1 2 3 15
16 17 18 19 31
32
48
64
80
N=72
120 : SHADED AREA B
(COLUMN VECTOR)
COLUMN
1151
130
READ
0 16 32 48 64 80 98 112 128 --- 1136 1 17 --- 2 18 ------ 15 31 --- 1151
INTERLEAVED DATA CONTAINED IN ONE FRAME

FIG. 2

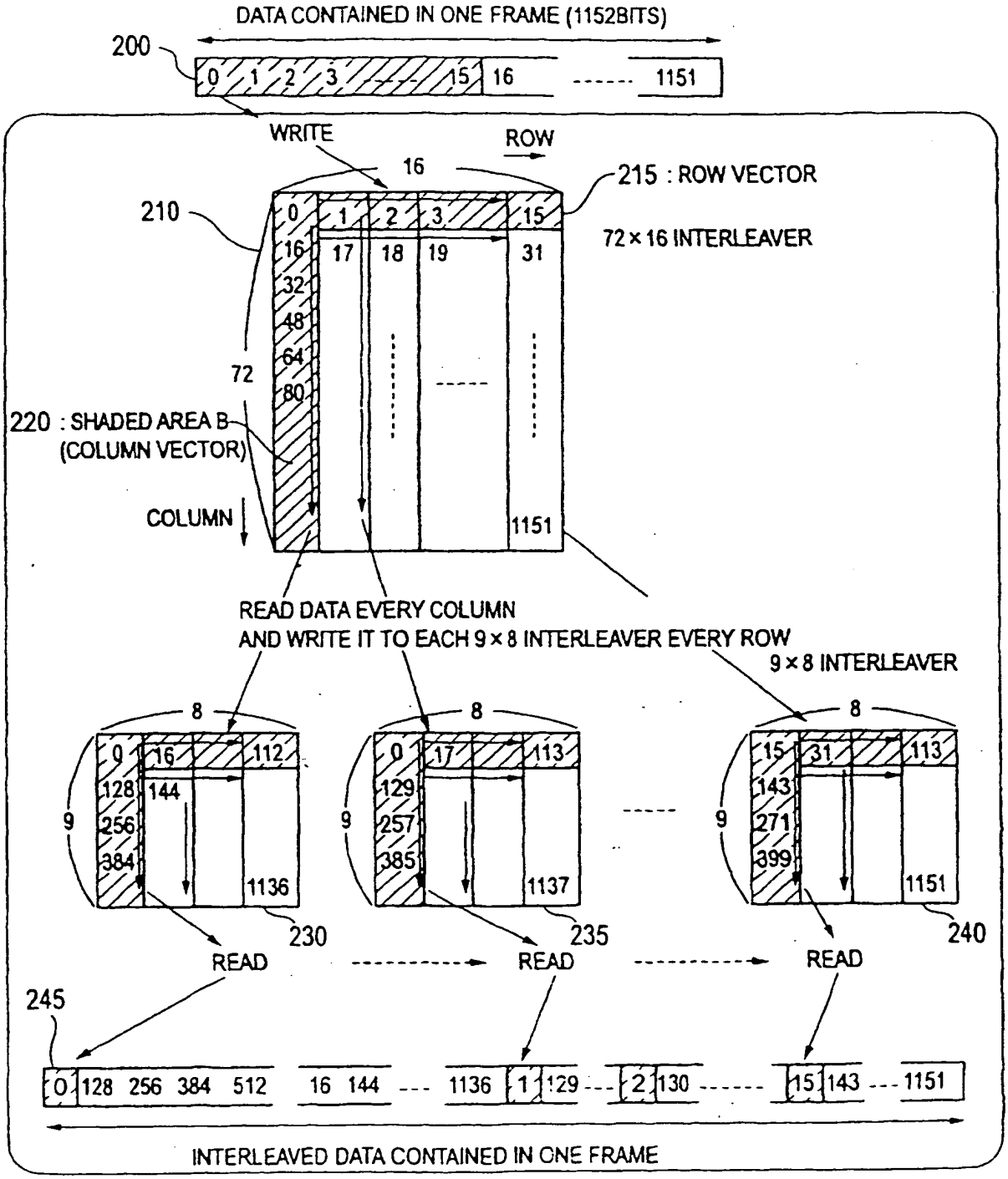

DATA CONTAINED IN ONE FRAME (1152BITS)
200
0 1 2 3 15 16 1151
WRITE
ROW
16
215 : ROW VECTOR
210
72 × 16 INTERLEAVER
72
220 : SHADED AREA B
(COLUMN VECTOR)
COLUMN
READ DATA EVERY COLUMN
AND WRITE IT TO EACH 9 × 8 INTERLEAVER EVERY ROW
9 × 8 INTERLEAVER
8
9
230
235
240
READ
245
INTERLEAVED DATA CONTAINED IN ONE FRAME

FIG. 3

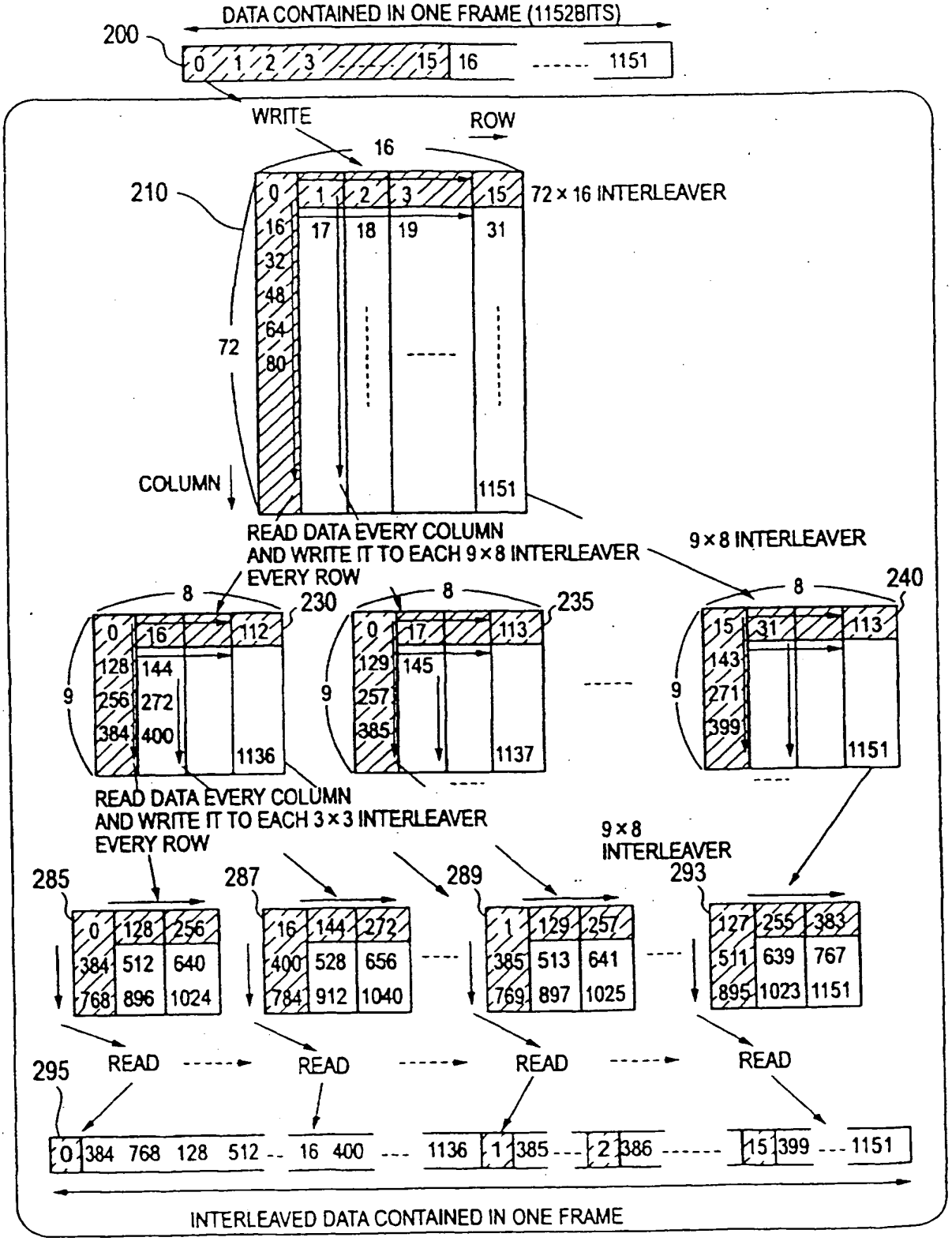

DATA CONTAINED IN ONE FRAME (1152BITS)
200
0 1 2 3 15 16 1151
WRITE
ROW
16
210
72 × 16 INTERLEAVER
72
COLUMN
READ DATA EVERY COLUMN AND WRITE IT TO EACH 9×8 INTERLEAVER EVERY ROW
9×8 INTERLEAVER
240
230
235
READ DATA EVERY COLUMN AND WRITE IT TO EACH 3×3 INTERLEAVER EVERY ROW
9×8 INTERLEAVER
285
287
289
293
READ
READ
READ
READ
295
INTERLEAVED DATA CONTAINED IN ONE FRAME

FIG. 4

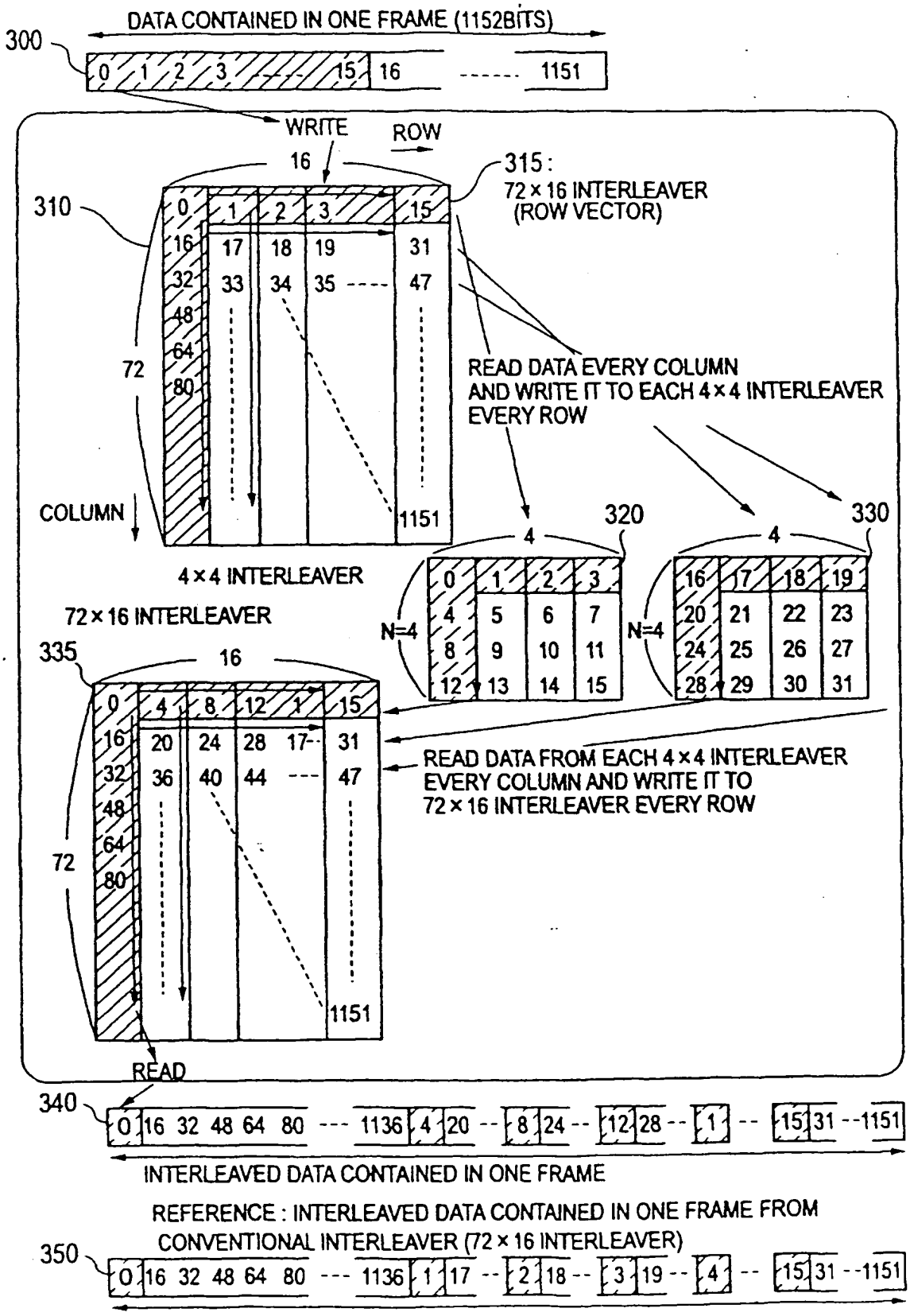

DATA CONTAINED IN ONE FRAME (1152BITS)
300
0 1 2 3 ---- 15 16 ------ 1151
WRITE
ROW
16
315 :
72 × 16 INTERLEAVER
(ROW VECTOR)
310
0 1 2 3 15
16 17 18 19 31
32 33 34 35 ---- 47
48
64
80
72
1151
READ DATA EVERY COLUMN
AND WRITE IT TO EACH 4 × 4 INTERLEAVER
EVERY ROW
COLUMN
4 × 4 INTERLEAVER
320
330
4
0 1 2 3
4 5 6 7
8 9 10 11
12 13 14 15
N=4
16 17 18 19
20 21 22 23
24 25 26 27
28 29 30 31
72 × 16 INTERLEAVER
335
0 4 8 12 1 15
16 20 24 28 17 31
32 36 40 44 --- 47
48
64
80
72
1151
READ DATA FROM EACH 4 × 4 INTERLEAVER
EVERY COLUMN AND WRITE IT TO
72 × 16 INTERLEAVER EVERY ROW
READ
340
0 16 32 48 64 80 --- 1136 4 20 -- 8 24 -- 12 28 -- 1 -- 15 31 --1151
INTERLEAVED DATA CONTAINED IN ONE FRAME
REFERENCE : INTERLEAVED DATA CONTAINED IN ONE FRAME FROM
CONVENTIONAL INTERLEAVER (72 × 16 INTERLEAVER)
350
0 16 32 48 64 80 --- 1136 1 17 -- 2 18 -- 3 19 -- 4 -- 15 31 --1151

FIG. 5

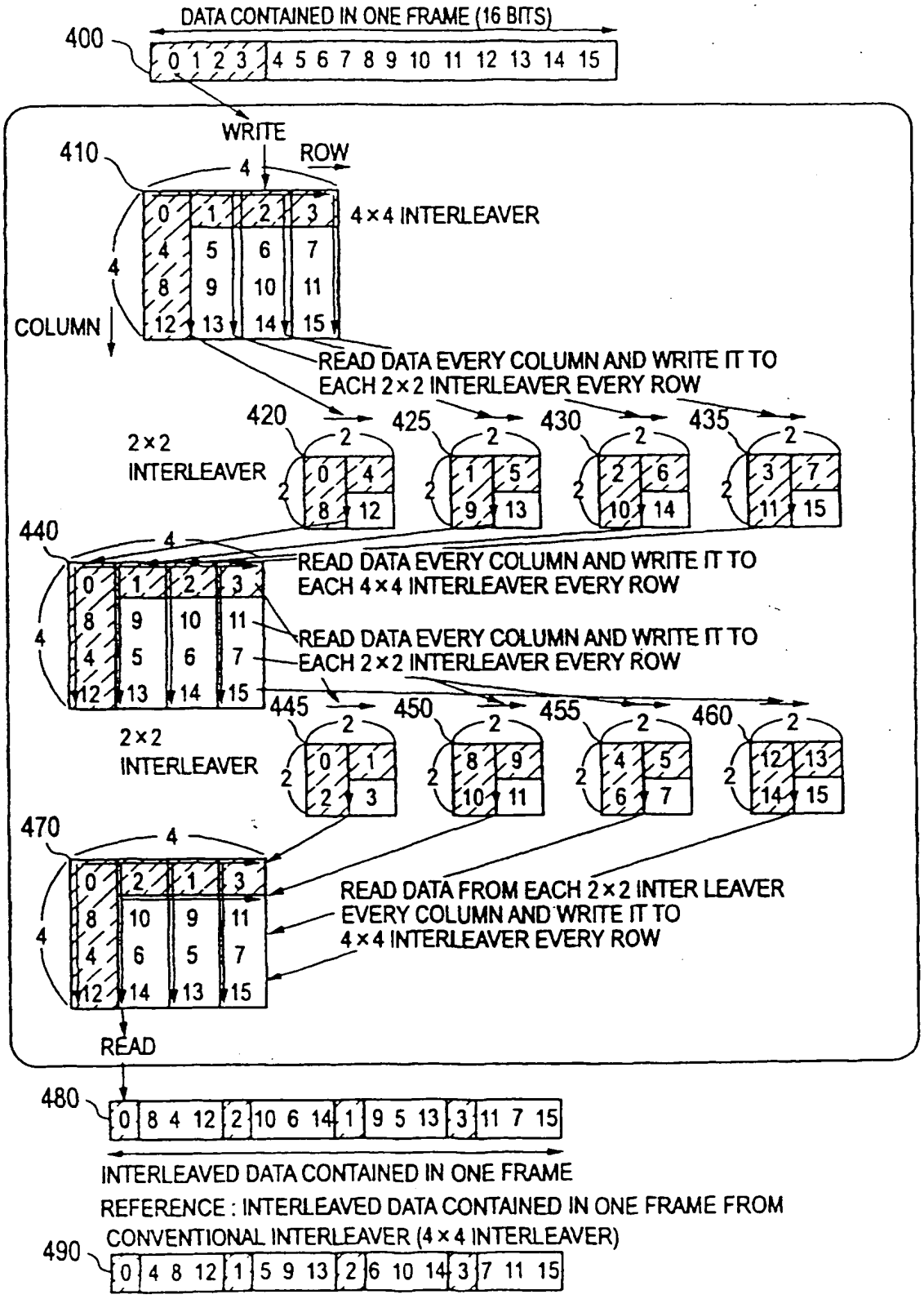

DATA CONTAINED IN ONE FRAME (16 BITS)
400
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
WRITE
ROW
COLUMN
410
4×4 INTERLEAVER
READ DATA EVERY COLUMN AND WRITE IT TO EACH 2×2 INTERLEAVER EVERY ROW
420
425
430
435
2×2 INTERLEAVER
440
READ DATA EVERY COLUMN AND WRITE IT TO EACH 4×4 INTERLEAVER EVERY ROW
READ DATA EVERY COLUMN AND WRITE IT TO EACH 2×2 INTERLEAVER EVERY ROW
445
450
455
460
2×2 INTERLEAVER
470
READ DATA FROM EACH 2×2 INTER LEAVER EVERY COLUMN AND WRITE IT TO 4×4 INTERLEAVER EVERY ROW
READ
480
0 8 4 12 2 10 6 14 1 9 5 13 3 11 7 15
INTERLEAVED DATA CONTAINED IN ONE FRAME
REFERENCE : INTERLEAVED DATA CONTAINED IN ONE FRAME FROM CONVENTIONAL INTERLEAVER (4×4 INTERLEAVER)
490
0 4 8 12 1 5 9 13 2 6 10 14 3 7 11 15

FIG. 6

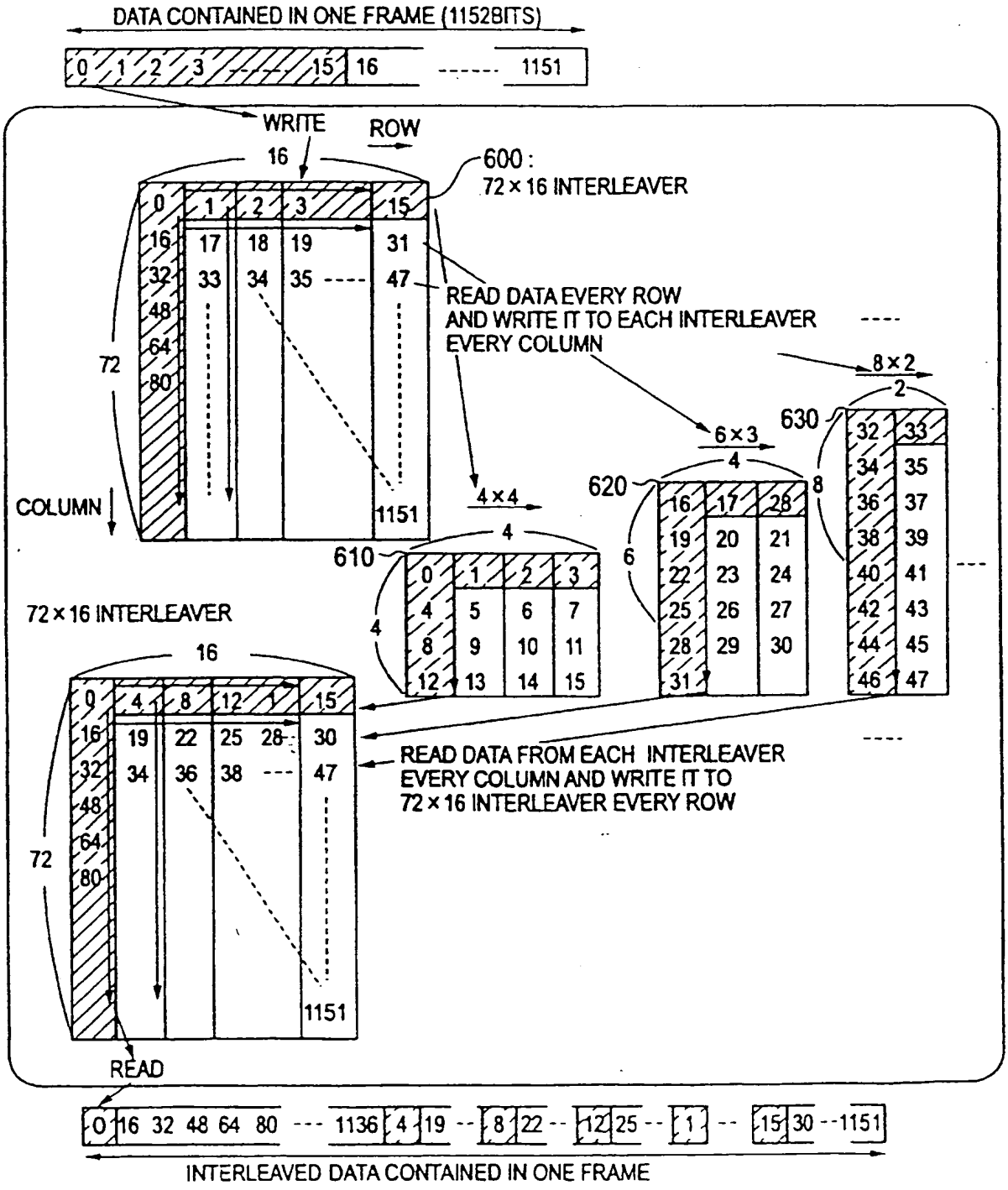

DATA CONTAINED IN ONE FRAME (1152BITS)
WRITE
ROW
600 :
72 × 16 INTERLEAVER
READ DATA EVERY ROW
AND WRITE IT TO EACH INTERLEAVER
EVERY COLUMN
COLUMN
72
4 × 4
610
6 × 3
620
8 × 2
630
72 × 16 INTERLEAVER
READ DATA FROM EACH INTERLEAVER
EVERY COLUMN AND WRITE IT TO
72 × 16 INTERLEAVER EVERY ROW
READ
INTERLEAVED DATA CONTAINED IN ONE FRAME

FIG. 7

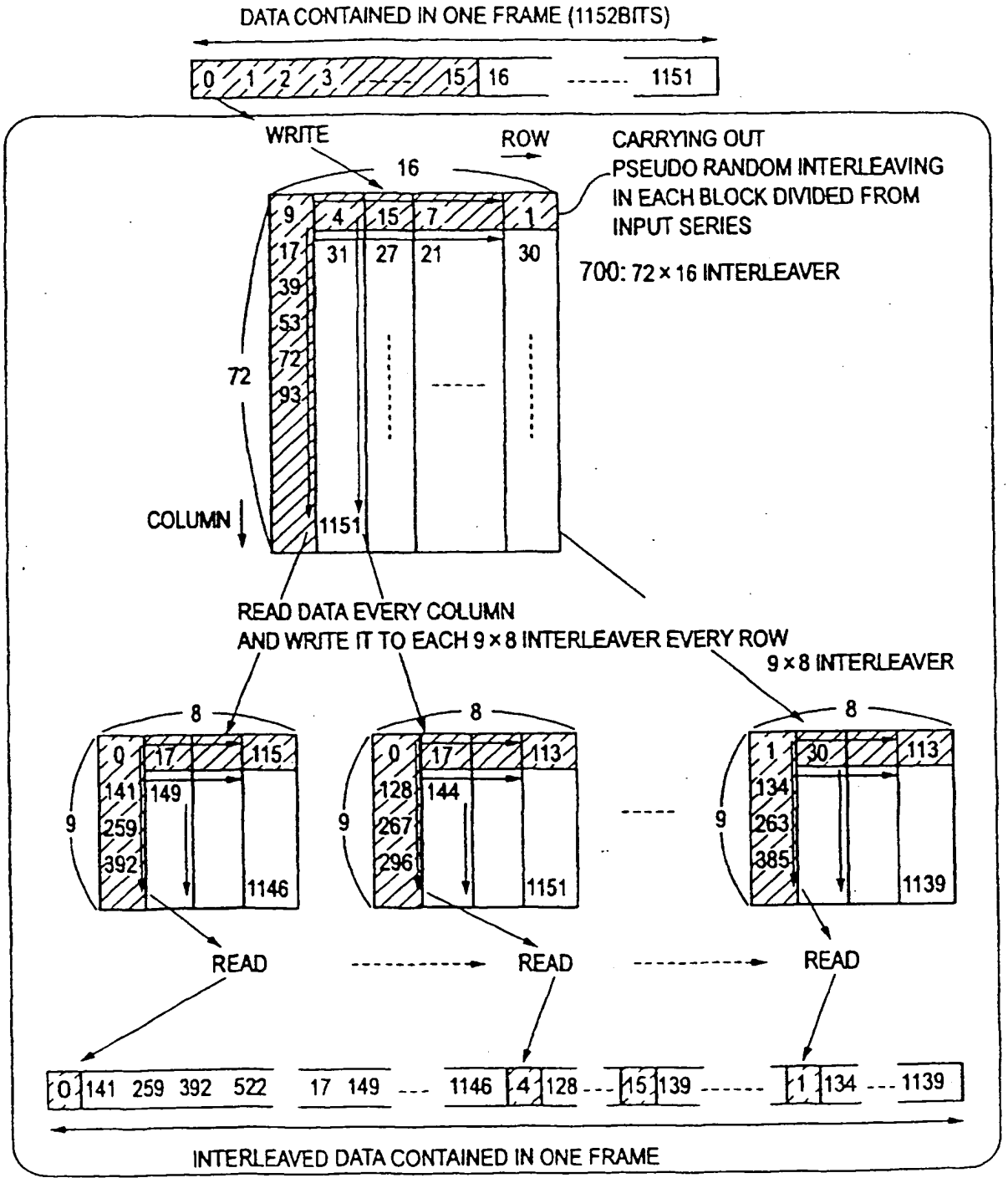

DATA CONTAINED IN ONE FRAME (1152BITS)
0 1 2 3 15 16 1151
WRITE
ROW
16
CARRYING OUT PSEUDO RANDOM INTERLEAVING IN EACH BLOCK DIVIDED FROM INPUT SERIES
700: 72 × 16 INTERLEAVER
9 4 15 7 1
17 31 27 21 30
39
53
72
93
72
COLUMN
1151
READ DATA EVERY COLUMN
AND WRITE IT TO EACH 9 × 8 INTERLEAVER EVERY ROW
9 × 8 INTERLEAVER
8
9
0 17 115
141 149
259
392
1146
0 17 113
128 144
267
296
1151
1 30 113
134
263
385
1139
READ
READ
READ
0 141 259 392 522 17 149 1146 4 128 15 139 1 134 1139
INTERLEAVED DATA CONTAINED IN ONE FRAME

FIG. 8

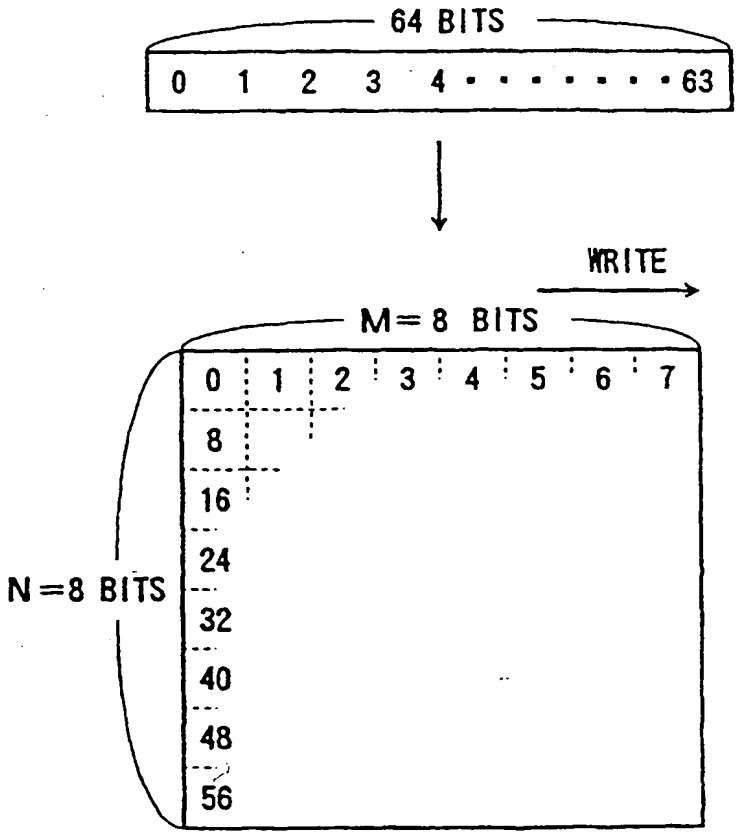

64 BITS
0 1 2 3 4 • • • • • • • 63
WRITE
M=8 BITS
0 1 2 3 4 5 6 7
8
16
24
32
40
48
56
N=8 BITS

FIG. 9

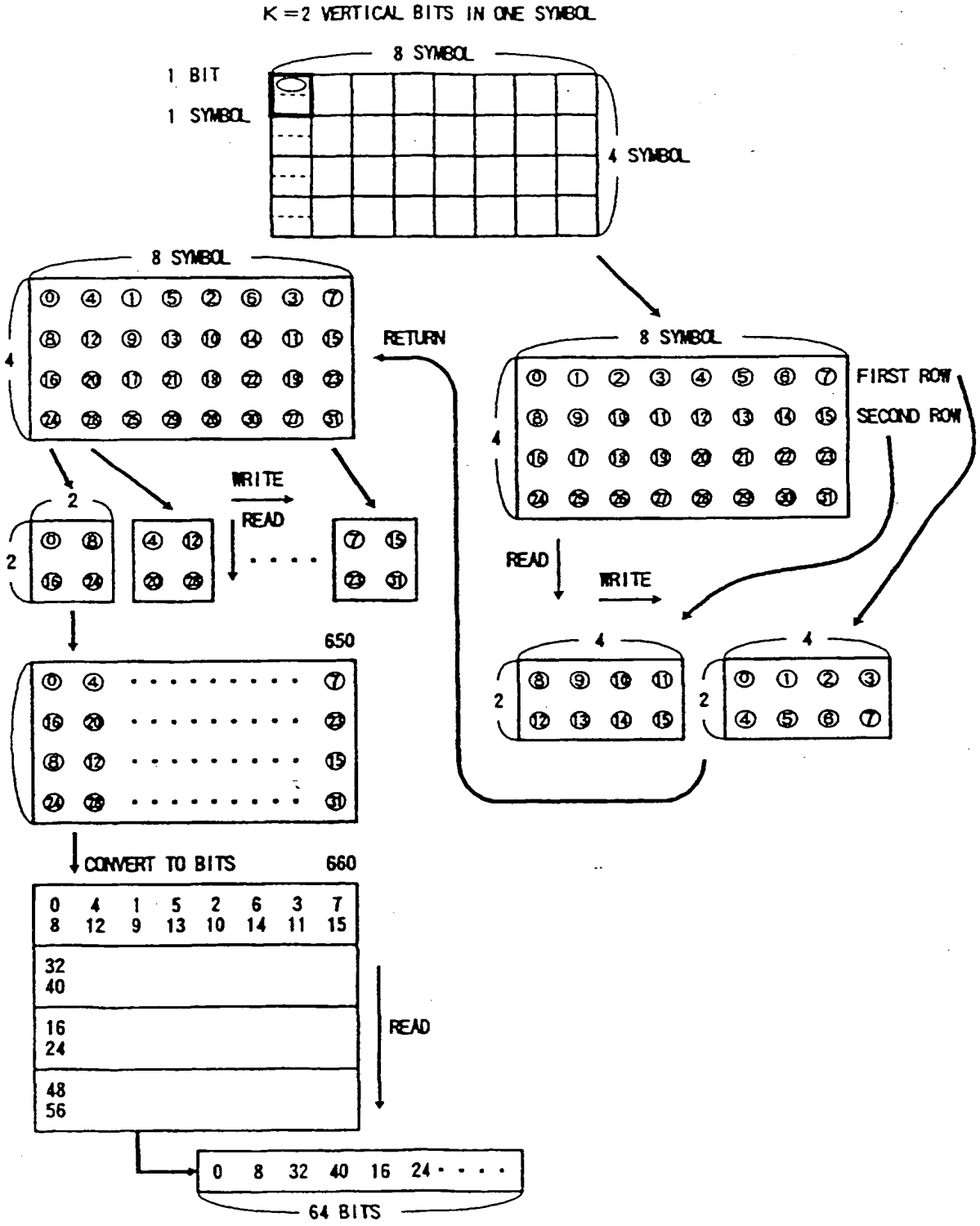

K=2 VERTICAL BITS IN ONE SYMBOL
8 SYMBOL
1 BIT
1 SYMBOL
4 SYMBOL
8 SYMBOL
RETURN
8 SYMBOL
FIRST ROW
SECOND ROW
WRITE
READ
READ
WRITE
650
CONVERT TO BITS
660
READ
64 BITS

FIG. 10

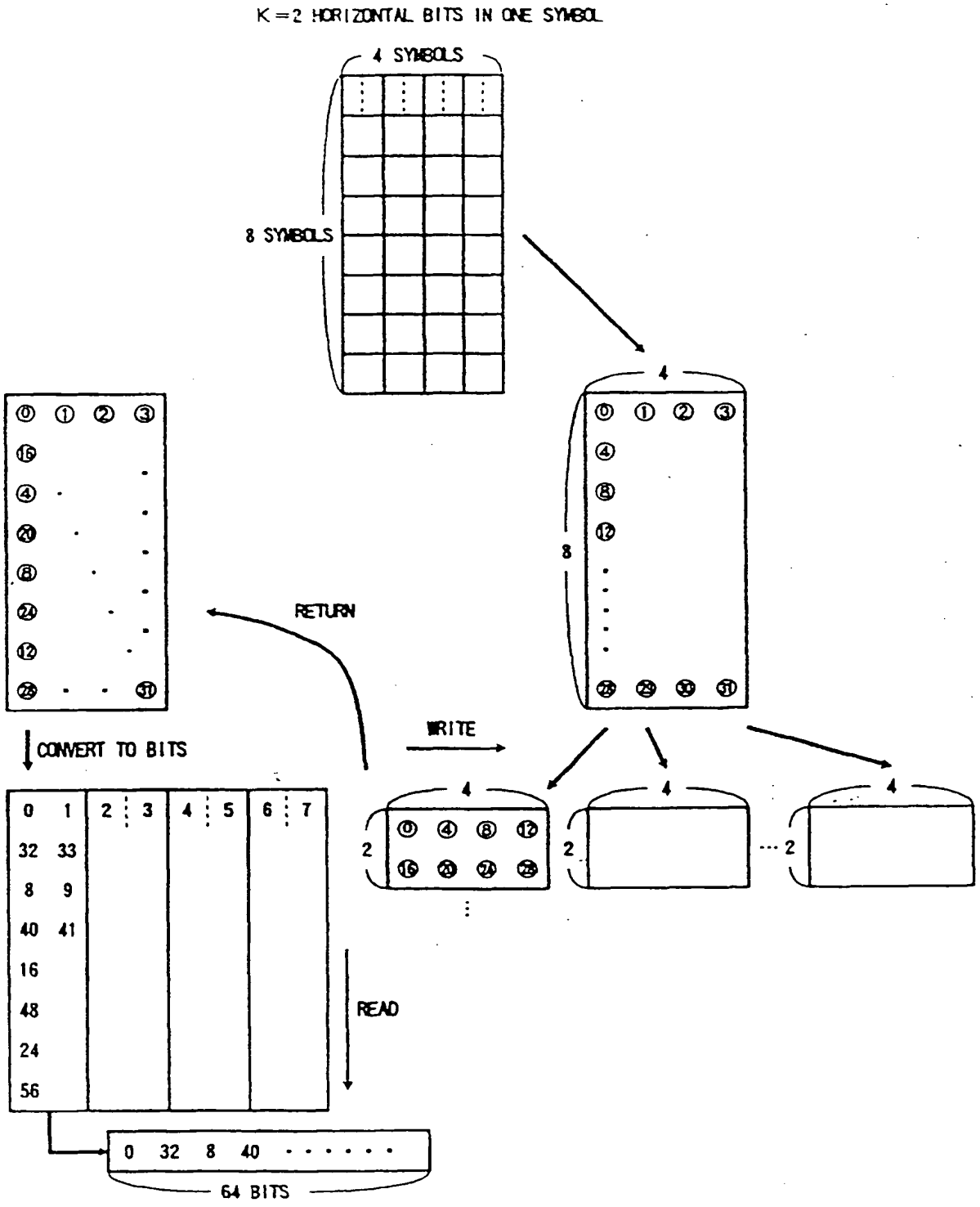

K=2 HORIZONTAL BITS IN ONE SYMBOL
4 SYMBOLS
8 SYMBOLS
4
8
RETURN
WRITE
CONVERT TO BITS
READ
2
2
2
0 1 2 3 4 5 6 7
32 33
8 9
40 41
16
48
24
56
0 32 8 40 . . . . . .
64 BITS

FIG. 11

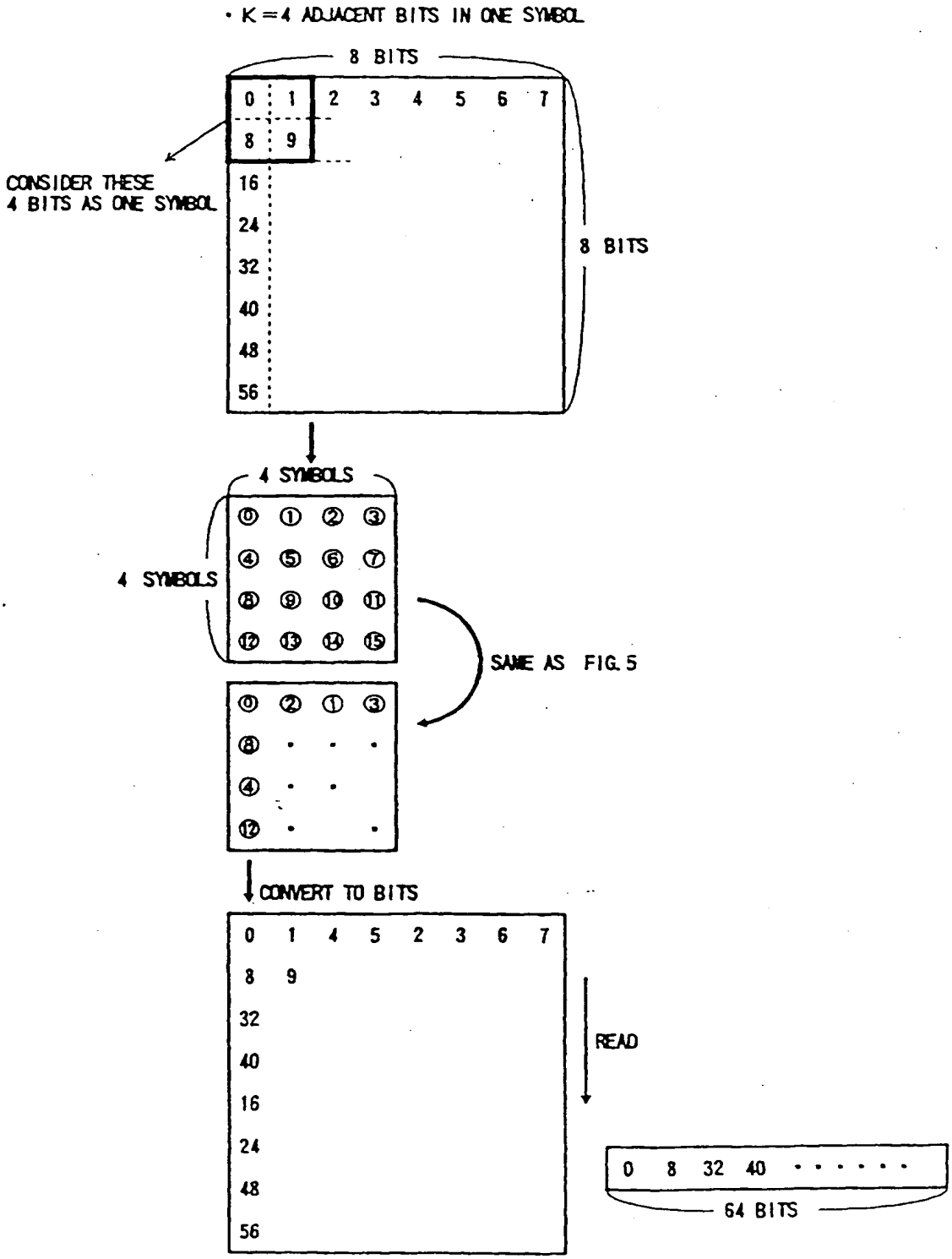

• K=4 ADJACENT BITS IN ONE SYMBOL
8 BITS
0 1 2 3 4 5 6 7
8 9
16
24
32
40
48
56
CONSIDER THESE 4 BITS AS ONE SYMBOL
8 BITS
4 SYMBOLS
⓪ ① ② ③
④ ⑤ ⑥ ⑦
⑧ ⑨ ⑩ ⑪
⑫ ⑬ ⑭ ⑮
4 SYMBOLS
SAME AS FIG. 5
⓪ ② ① ③
⑧ • • •
④ • •
⑫ • •
CONVERT TO BITS
0 1 4 5 2 3 6 7
8 9
32
40
16
24
48
56
READ
0 8 32 40 • • • • • •
64 BITS

FIG. 12

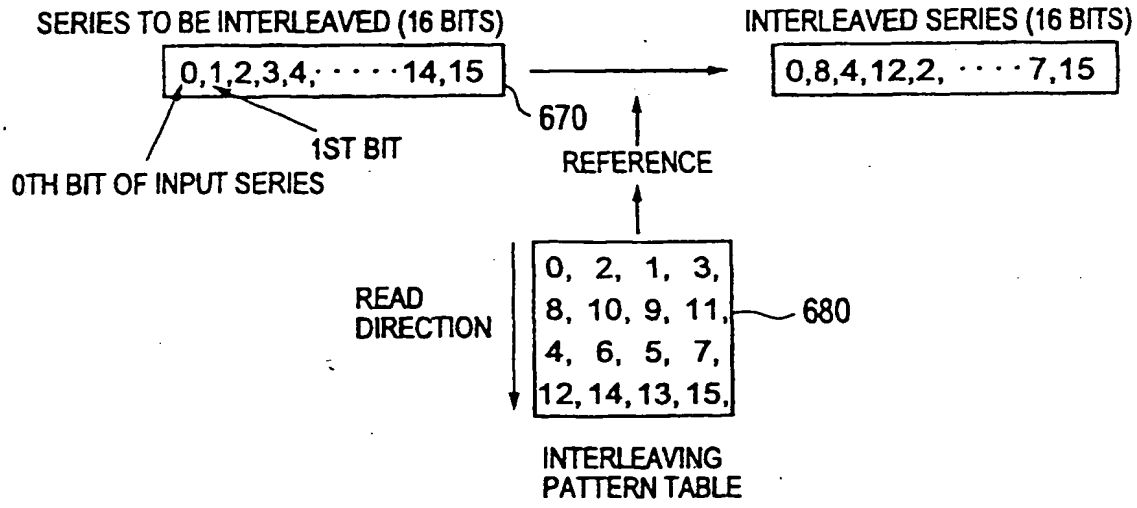

SERIES TO BE INTERLEAVED (16 BITS)
0,1,2,3,4,· · · ·14,15
INTERLEAVED SERIES (16 BITS)
0,8,4,12,2, · · · ·7,15
670
1ST BIT
0TH BIT OF INPUT SERIES
REFERENCE
READ DIRECTION
0, 2, 1, 3,
8, 10, 9, 11,
4, 6, 5, 7,
12, 14, 13, 15,
680
INTERLEAVING PATTERN TABLE

FIG. 13

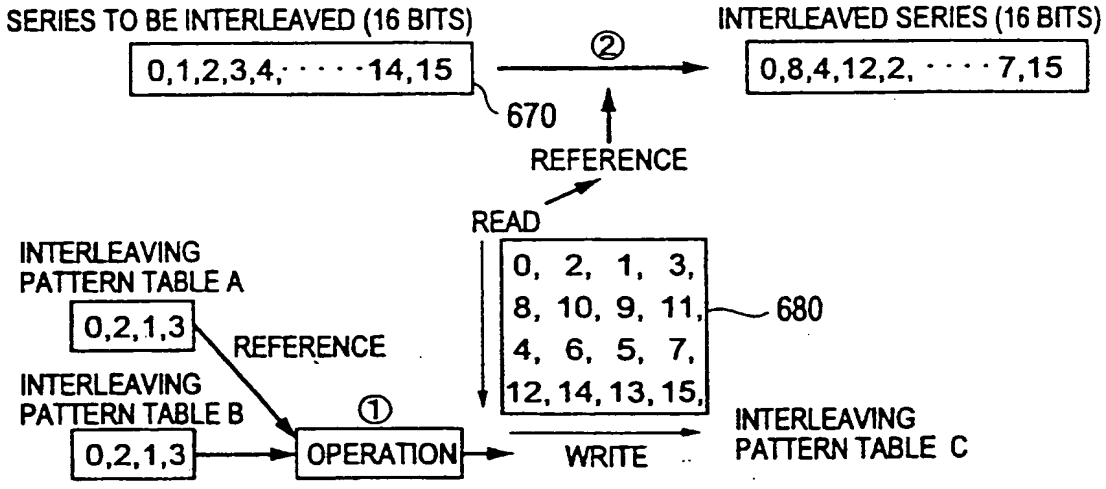

SERIES TO BE INTERLEAVED (16 BITS)
0,1,2,3,4,· · · · ·14,15
670
②
INTERLEAVED SERIES (16 BITS)
0,8,4,12,2, · · · · 7,15
REFERENCE
READ
INTERLEAVING PATTERN TABLE A
0,2,1,3
REFERENCE
INTERLEAVING PATTERN TABLE B
0,2,1,3
①
OPERATION
0, 2, 1, 3,
8, 10, 9, 11,
4, 6, 5, 7,
12, 14, 13, 15,
680
WRITE
INTERLEAVING PATTERN TABLE C

FIG. 14

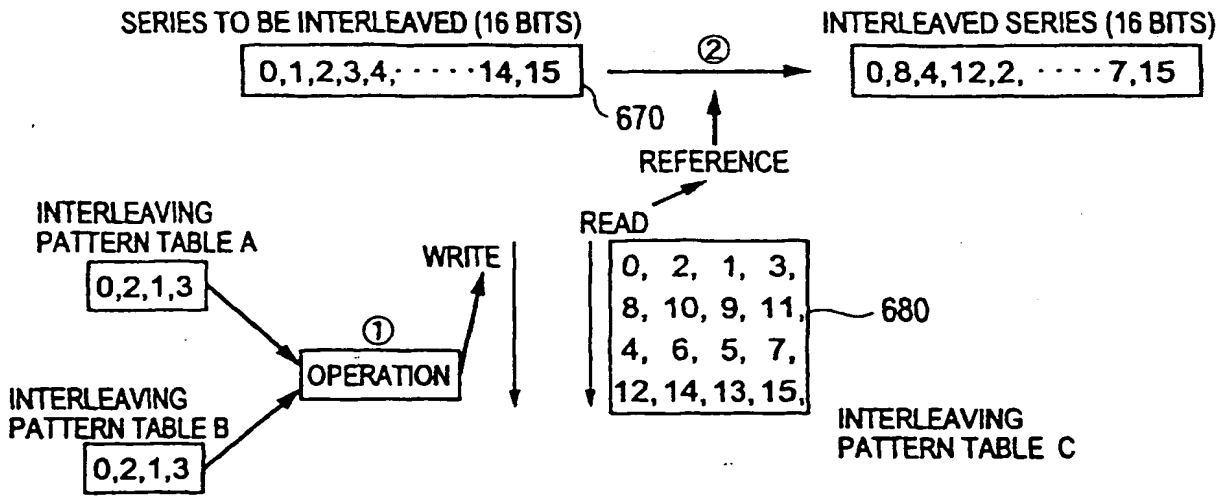

SERIES TO BE INTERLEAVED (16 BITS)
0,1,2,3,4,· · · ·14,15
670
②
INTERLEAVED SERIES (16 BITS)
0,8,4,12,2, · · · ·7,15
REFERENCE
READ
WRITE
INTERLEAVING PATTERN TABLE A
0,2,1,3
①
OPERATION
INTERLEAVING PATTERN TABLE B
0,2,1,3
0, 2, 1, 3,
8, 10, 9, 11,
4, 6, 5, 7,
12, 14, 13, 15,
680
INTERLEAVING PATTERN TABLE C

FIG. 15

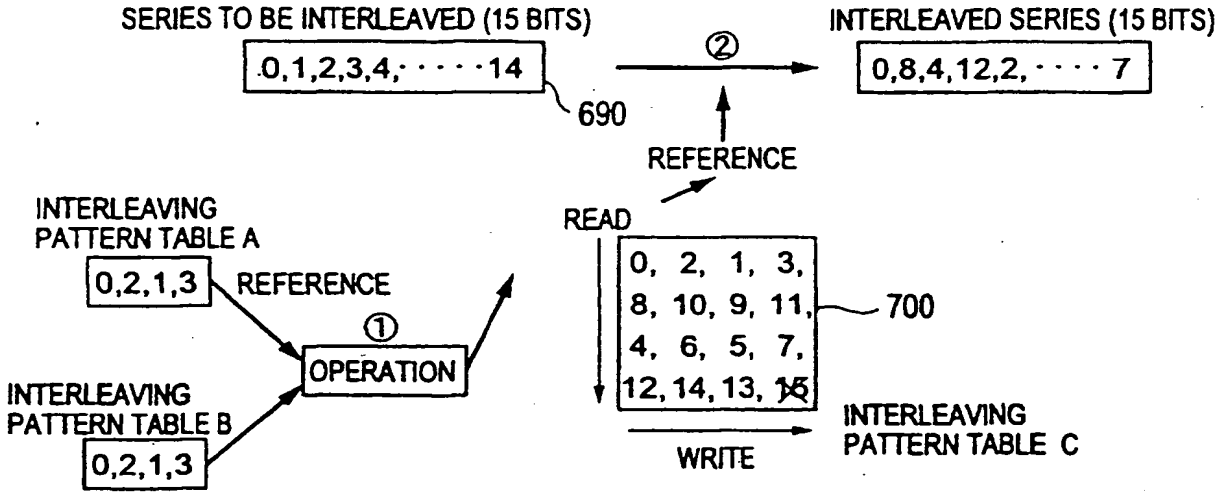

SERIES TO BE INTERLEAVED (15 BITS)
0,1,2,3,4,· · · · ·14
690
②
INTERLEAVED SERIES (15 BITS)
0,8,4,12,2,· · · · 7
REFERENCE
READ
INTERLEAVING PATTERN TABLE A
0,2,1,3
REFERENCE
①
OPERATION
INTERLEAVING PATTERN TABLE B
0,2,1,3
0, 2, 1, 3,
8, 10, 9, 11,
4, 6, 5, 7,
12, 14, 13, 15
700
WRITE
INTERLEAVING PATTERN TABLE C

FIG. 16

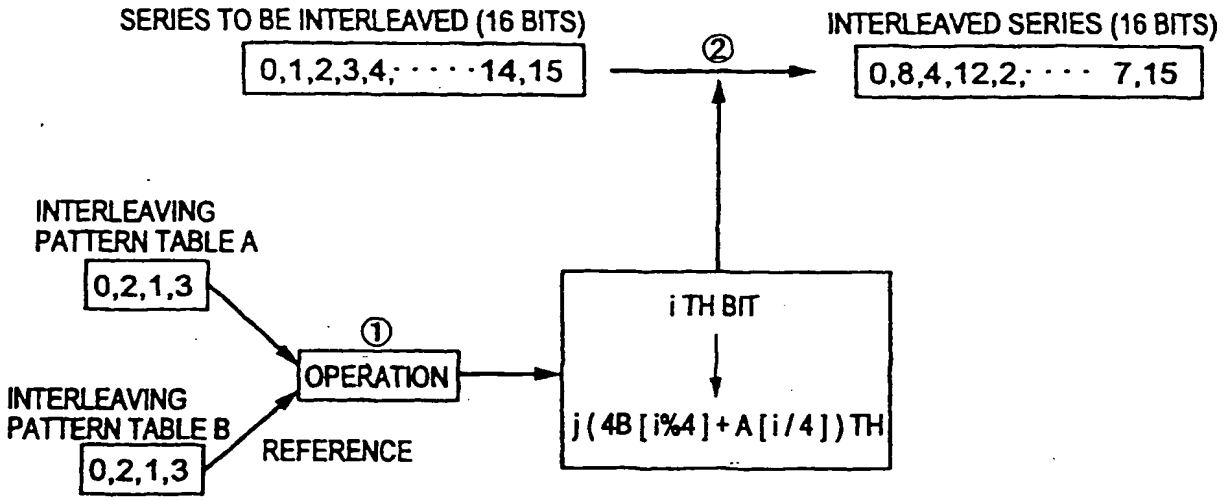

SERIES TO BE INTERLEAVED (16 BITS)
0,1,2,3,4,· · · · ·14,15
②
INTERLEAVED SERIES (16 BITS)
0,8,4,12,2,· · · · 7,15
INTERLEAVING PATTERN TABLE A
0,2,1,3
①
OPERATION
INTERLEAVING PATTERN TABLE B
0,2,1,3
REFERENCE
i TH BIT
j (4B [i%4] + A [i/4]) TH

FIG. 17

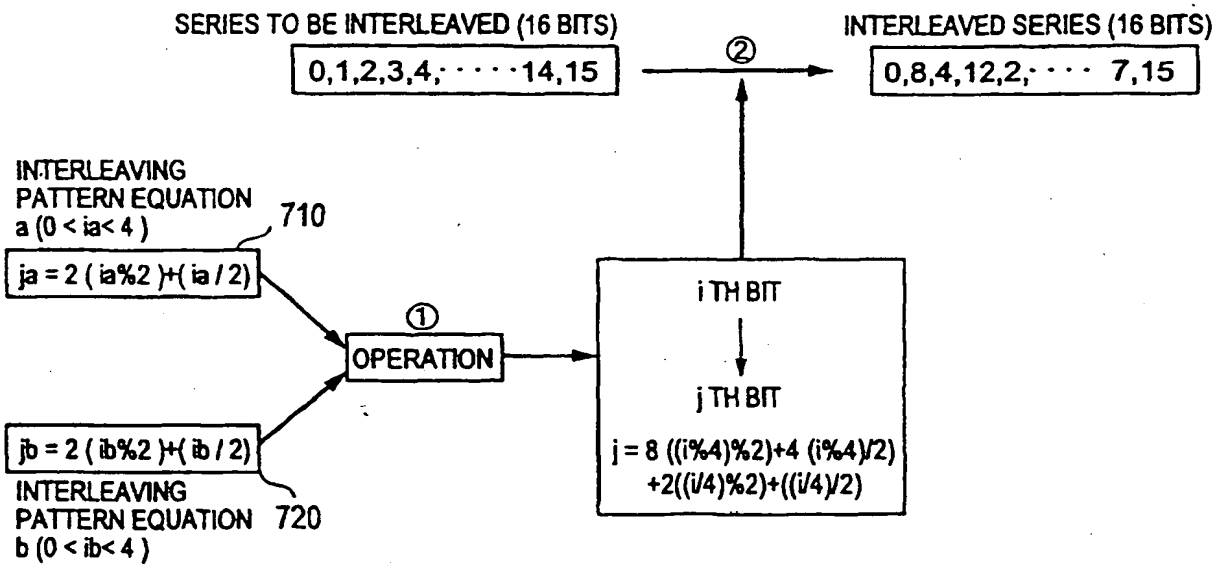

SERIES TO BE INTERLEAVED (16 BITS)
0,1,2,3,4,· · · · ·14,15
②
INTERLEAVED SERIES (16 BITS)
0,8,4,12,2,· · · · 7,15
INTERLEAVING PATTERN EQUATION a (0 < ia< 4)
710
ja = 2 (ia%2)+(ia / 2)
①
OPERATION
i TH BIT
j TH BIT
j = 8 ((i%4)%2)+4 (i%4)/2) +2((i/4)%2)+((i/4)/2)
jb = 2 (ib%2)+(ib / 2)
INTERLEAVING PATTERN EQUATION
720
b (0 < ib< 4)

FIG. 18

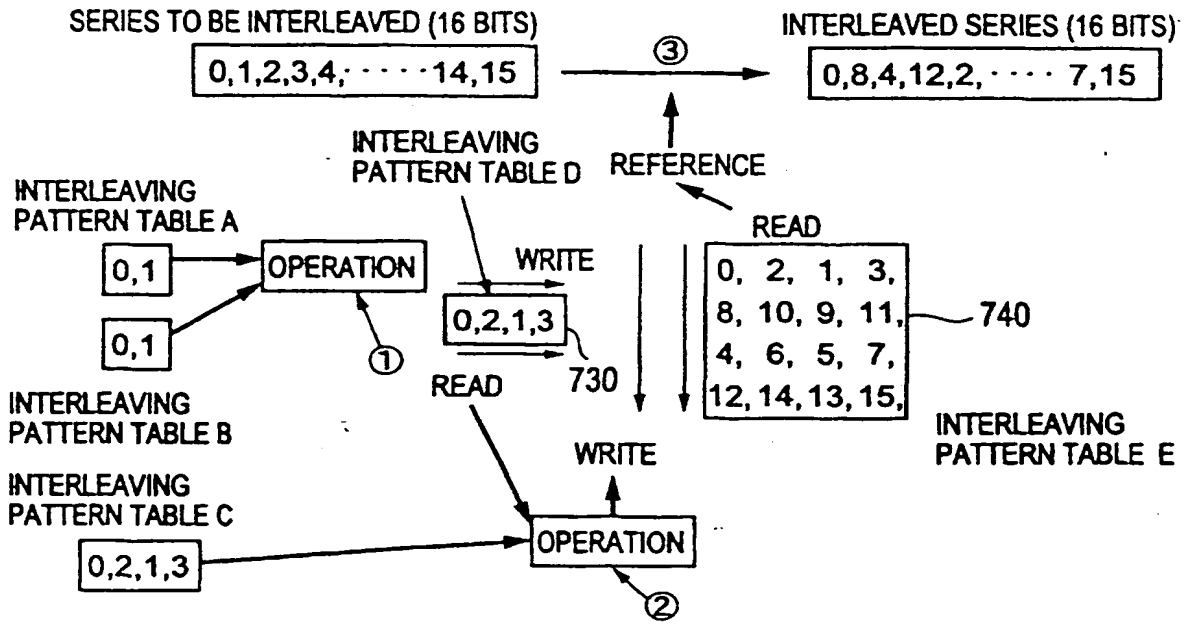

SERIES TO BE INTERLEAVED (16 BITS)
0,1,2,3,4,· · · · ·14,15
③
INTERLEAVED SERIES (16 BITS)
0,8,4,12,2,· · · · 7,15
INTERLEAVING PATTERN TABLE D
REFERENCE
INTERLEAVING PATTERN TABLE A
0,1
OPERATION
WRITE
0,2,1,3
730
READ
0, 2, 1, 3,
8, 10, 9, 11,
4, 6, 5, 7,
12, 14, 13, 15,
740
INTERLEAVING PATTERN TABLE E
①
0,1
INTERLEAVING PATTERN TABLE B
WRITE
INTERLEAVING PATTERN TABLE C
0,2,1,3
OPERATION
②

FIG. 19

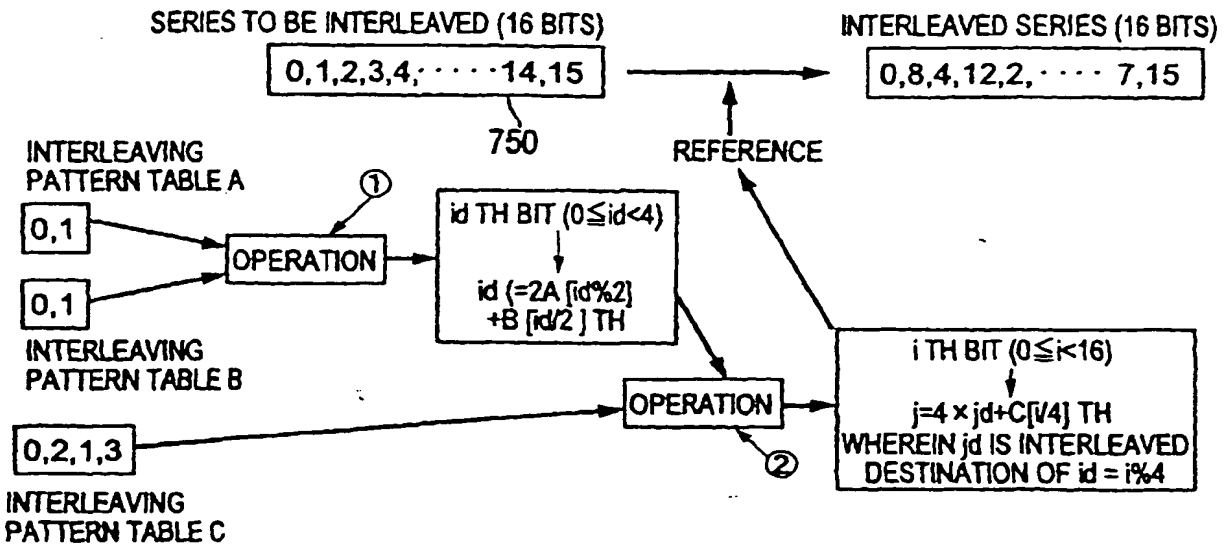

SERIES TO BE INTERLEAVED (16 BITS)
0,1,2,3,4,· · · · ·14,15
750
INTERLEAVED SERIES (16 BITS)
0,8,4,12,2,· · · · 7,15
REFERENCE
INTERLEAVING PATTERN TABLE A
0,1
0,1
INTERLEAVING PATTERN TABLE B
0,2,1,3
INTERLEAVING PATTERN TABLE C
OPERATION
①
id TH BIT (0≦id<4)
id (=2A [id%2] +B [id/2] TH
OPERATION
②
i TH BIT (0≦i<16)
j=4 × jd+C[i/4] TH
WHEREIN jd IS INTERLEAVED DESTINATION OF id = i%4

FIG.20

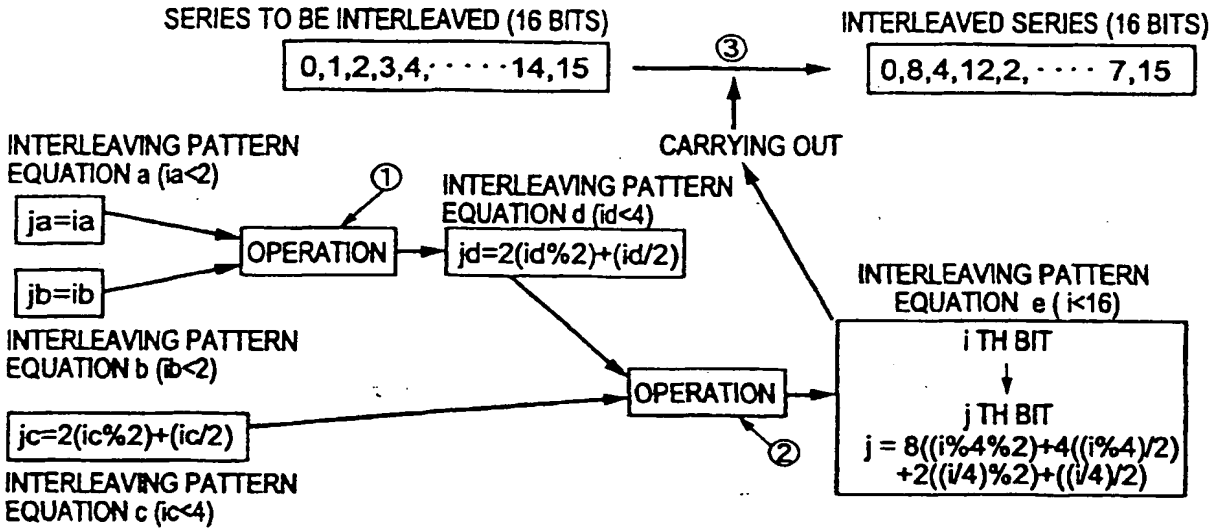

SERIES TO BE INTERLEAVED (16 BITS)
0,1,2,3,4,· · · · ·14,15
③
INTERLEAVED SERIES (16 BITS)
0,8,4,12,2,· · · · 7,15
CARRYING OUT
INTERLEAVING PATTERN EQUATION a (ia<2)
ja=ia
①
OPERATION
INTERLEAVING PATTERN EQUATION d (id<4)
jd=2(id%2)+(id/2)
jb=ib
INTERLEAVING PATTERN EQUATION b (ib<2)
INTERLEAVING PATTERN EQUATION e (i<16)
i TH BIT
OPERATION
j TH BIT
j = 8((i%4%2)+4((i%4)/2) +2((i/4)%2)+((i/4)/2)
②
jc=2(ic%2)+(ic/2)
INTERLEAVING PATTERN EQUATION c (ic<4)

FIG. 21

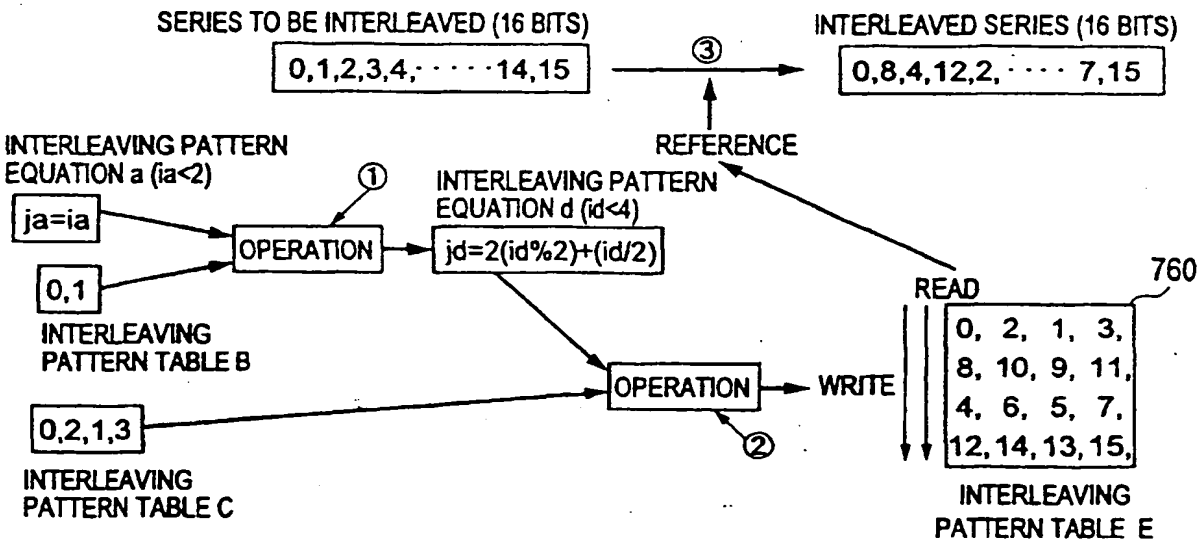

SERIES TO BE INTERLEAVED (16 BITS)
0,1,2,3,4,· · · · ·14,15
③
INTERLEAVED SERIES (16 BITS)
0,8,4,12,2,· · · · 7,15
REFERENCE
INTERLEAVING PATTERN EQUATION a (ia<2)
①
INTERLEAVING PATTERN EQUATION d (id<4)
ja=ia
OPERATION
jd=2(id%2)+(id/2)
0,1
INTERLEAVING PATTERN TABLE B
READ
760
OPERATION
WRITE
0,2,1,3
②
0, 2, 1, 3,
8, 10, 9, 11,
4, 6, 5, 7,
12, 14, 13, 15,
INTERLEAVING PATTERN TABLE C
INTERLEAVING PATTERN TABLE E

FIG. 22

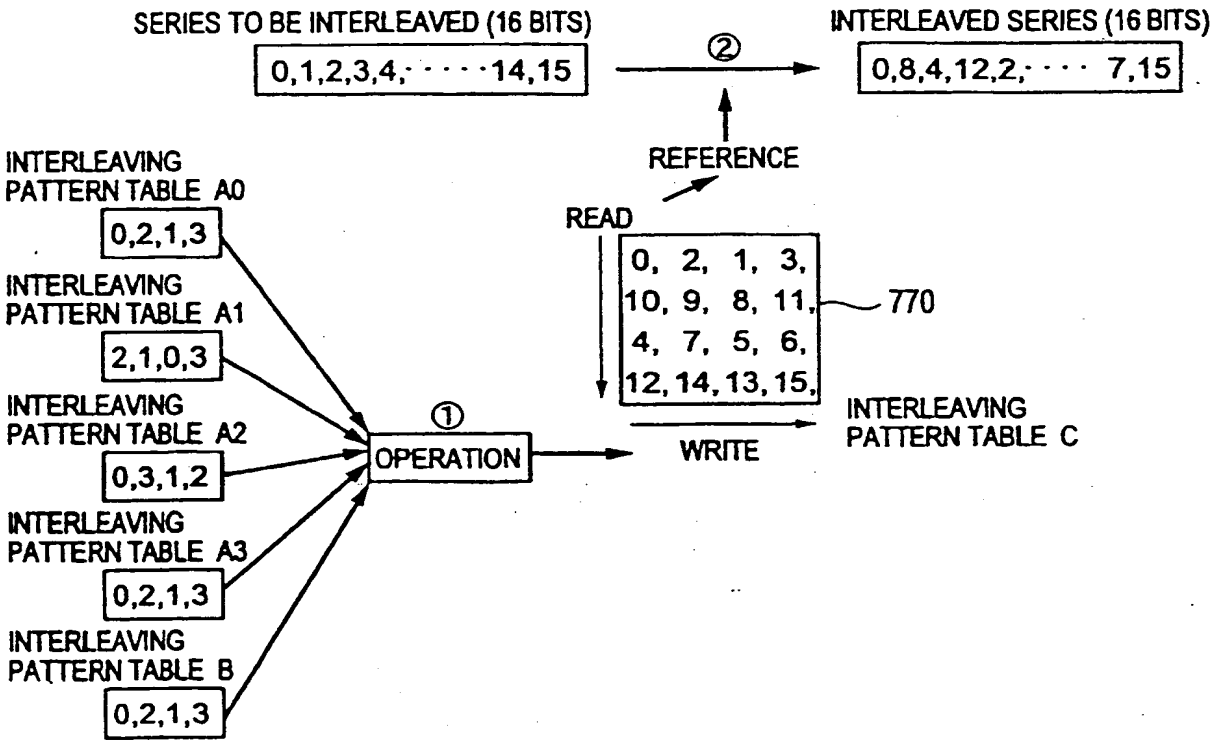

SERIES TO BE INTERLEAVED (16 BITS)
0,1,2,3,4,· · · · ·14,15
②
INTERLEAVED SERIES (16 BITS)
0,8,4,12,2,· · · · 7,15
REFERENCE
READ
INTERLEAVING PATTERN TABLE A0
0,2,1,3
INTERLEAVING PATTERN TABLE A1
2,1,0,3
INTERLEAVING PATTERN TABLE A2
0,3,1,2
INTERLEAVING PATTERN TABLE A3
0,2,1,3
INTERLEAVING PATTERN TABLE B
0,2,1,3
①
OPERATION
0, 2, 1, 3,
10, 9, 8, 11,
4, 7, 5, 6,
12, 14, 13, 15,
770
WRITE
INTERLEAVING PATTERN TABLE C

FIG. 23

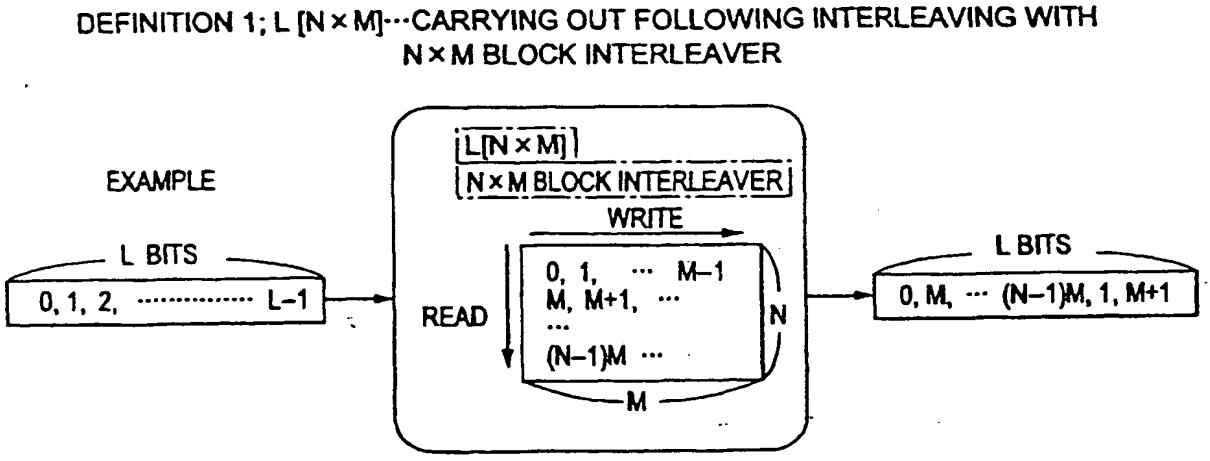

DEFINITION 1; L [N × M]···CARRYING OUT FOLLOWING INTERLEAVING WITH N × M BLOCK INTERLEAVER
EXAMPLE
L BITS
0, 1, 2, ····· L–1
L[N × M]
N × M BLOCK INTERLEAVER
WRITE
READ
0, 1, ··· M–1
M, M+1, ···
···
(N–1)M ···
N
M
L BITS
0, M, ··· (N–1)M, 1, M+1

FIG.24

DEFINITION 2; R { A } ···REARRANGING IN INVERSE ORDER

EXAMPLE

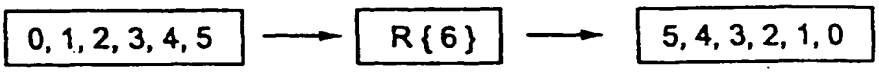


FIG.25

DEFINITION 3 ; L [N1 × M1, N2 × M2···] ··· INTERLEAVING WITH INTERLEAVER CORRESPONDING TO EACH OF A PLURALITY OF SERIES
(EACH SERIES IS L BITS)

EXAMPLE

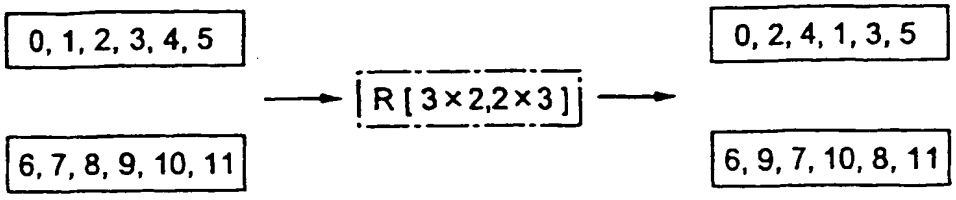


FIG. 27

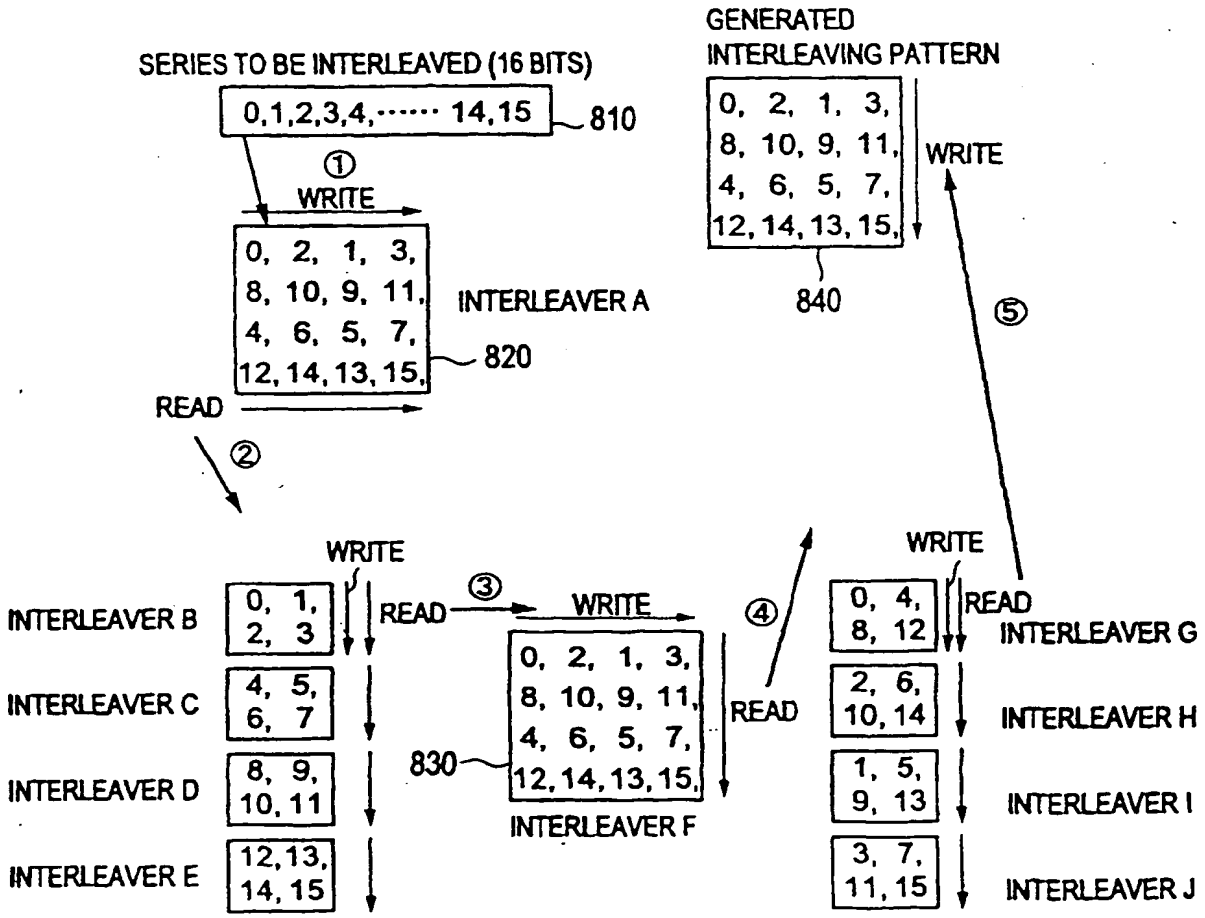

SERIES TO BE INTERLEAVED (16 BITS)
0,1,2,3,4,····· 14,15
810
①
WRITE
0, 2, 1, 3,
8, 10, 9, 11,
4, 6, 5, 7,
12, 14, 13, 15,
INTERLEAVER A
820
READ
②
GENERATED
INTERLEAVING PATTERN
0, 2, 1, 3,
8, 10, 9, 11,
4, 6, 5, 7,
12, 14, 13, 15,
840
WRITE
⑤
WRITE
INTERLEAVER B
0, 1,
2, 3
READ
③
WRITE
INTERLEAVER C
4, 5,
6, 7
INTERLEAVER D
8, 9,
10, 11
INTERLEAVER E
12, 13,
14, 15
0, 2, 1, 3,
8, 10, 9, 11,
4, 6, 5, 7,
12, 14, 13, 15,
830
INTERLEAVER F
READ
④
WRITE
0, 4,
8, 12
READ
INTERLEAVER G
2, 6,
10, 14
INTERLEAVER H
1, 5,
9, 13
INTERLEAVER I
3, 7,
11, 15
INTERLEAVER J

FIG. 28

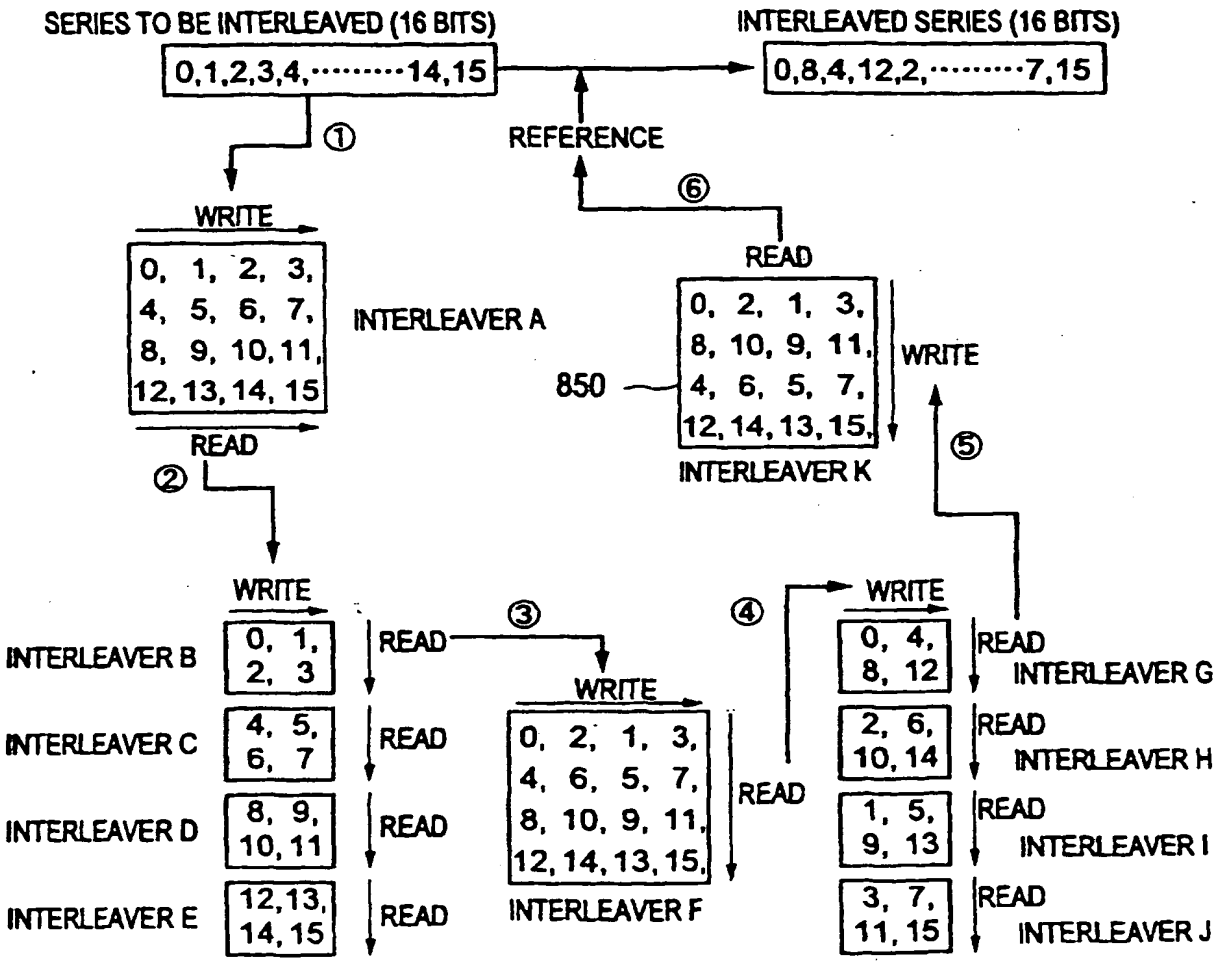

SERIES TO BE INTERLEAVED (16 BITS)
0,1,2,3,4,·····14,15
INTERLEAVED SERIES (16 BITS)
0,8,4,12,2,·····7,15
①
REFERENCE
⑥
WRITE
0, 1, 2, 3,
4, 5, 6, 7,
8, 9, 10, 11,
12, 13, 14, 15
INTERLEAVER A
READ
0, 2, 1, 3,
8, 10, 9, 11,
4, 6, 5, 7,
12, 14, 13, 15,
850
INTERLEAVER K
WRITE
READ
②
⑤
WRITE
INTERLEAVER B
0, 1,
2, 3
READ
③
WRITE
④
WRITE
0, 4,
8, 12
READ
INTERLEAVER G
INTERLEAVER C
4, 5,
6, 7
READ
0, 2, 1, 3,
4, 6, 5, 7,
8, 10, 9, 11,
12, 14, 13, 15,
READ
2, 6,
10, 14
READ
INTERLEAVER H
INTERLEAVER D
8, 9,
10, 11
READ
1, 5,
9, 13
READ
INTERLEAVER I
INTERLEAVER E
12, 13,
14, 15
READ
INTERLEAVER F
3, 7,
11, 15
READ
INTERLEAVER J

FIG.29

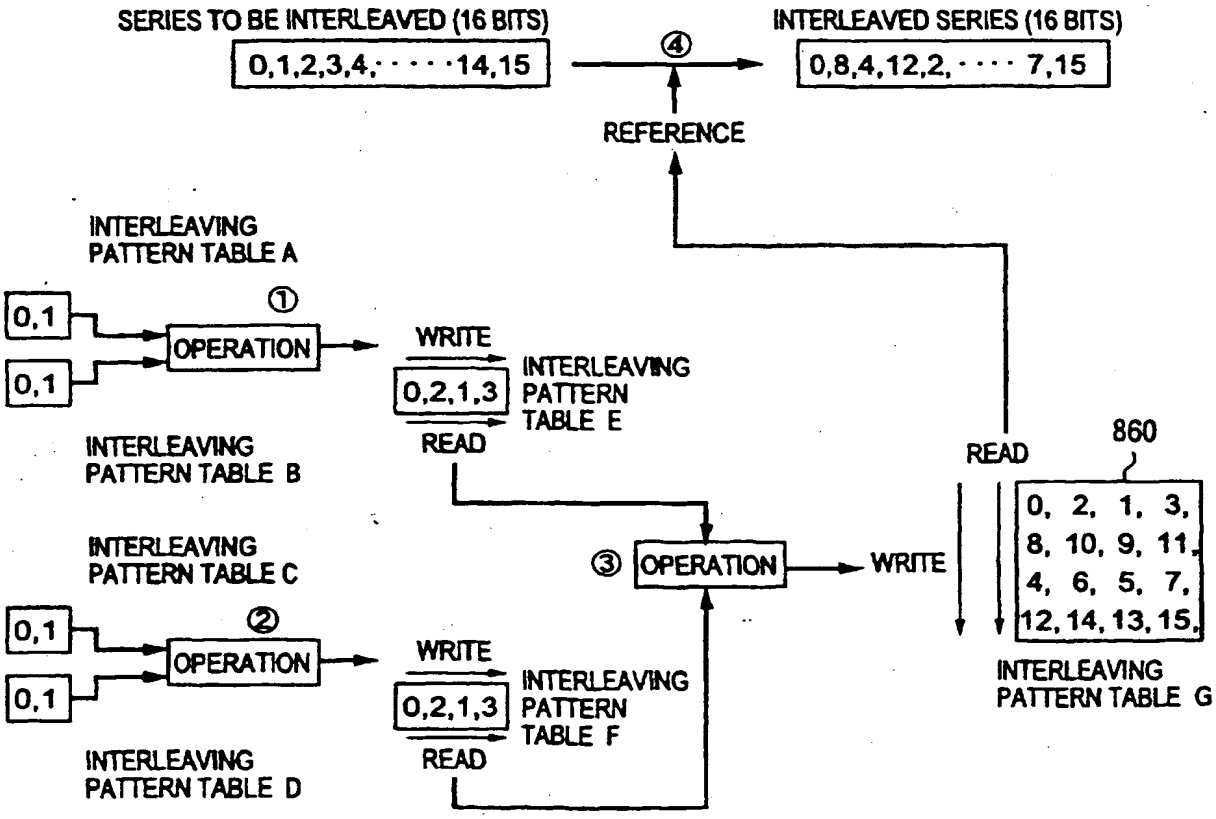

SERIES TO BE INTERLEAVED (16 BITS)
0,1,2,3,4,· · · · ·14,15
④
INTERLEAVED SERIES (16 BITS)
0,8,4,12,2,· · · · 7,15
REFERENCE
INTERLEAVING PATTERN TABLE A
①
0,1
0,1
OPERATION
WRITE
0,2,1,3
INTERLEAVING PATTERN TABLE E
READ
INTERLEAVING PATTERN TABLE B
INTERLEAVING PATTERN TABLE C
③ OPERATION
WRITE
READ
860
0, 2, 1, 3,
8, 10, 9, 11,
4, 6, 5, 7,
12, 14, 13, 15,
INTERLEAVING PATTERN TABLE G
②
0,1
0,1
OPERATION
WRITE
0,2,1,3
INTERLEAVING PATTERN TABLE F
READ
INTERLEAVING PATTERN TABLE D

FIG.30

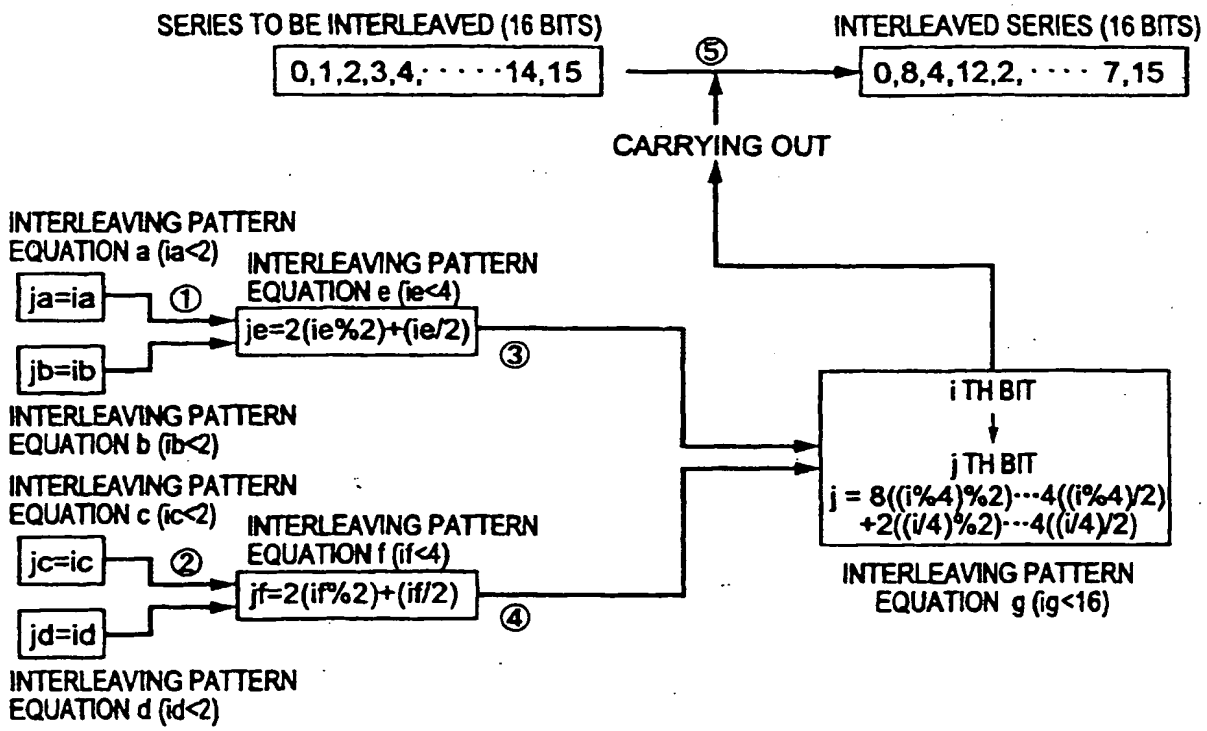

SERIES TO BE INTERLEAVED (16 BITS)
0,1,2,3,4,· · · ·14,15
⑤
INTERLEAVED SERIES (16 BITS)
0,8,4,12,2,· · · · 7,15
CARRYING OUT
INTERLEAVING PATTERN EQUATION a (ia<2)
ja=ia
①
INTERLEAVING PATTERN EQUATION e (ie<4)
je=2(ie%2)+(ie/2)
③
jb=ib
INTERLEAVING PATTERN EQUATION b (ib<2)
INTERLEAVING PATTERN EQUATION c (ic<2)
jc=ic
②
INTERLEAVING PATTERN EQUATION f (if<4)
jf=2(if%2)+(if/2)
④
jd=id
INTERLEAVING PATTERN EQUATION d (id<2)
i TH BIT
j TH BIT
j = 8((i%4)%2)···4((i%4)/2)
+2((i/4)%2)···4((i/4)/2)
INTERLEAVING PATTERN EQUATION g (ig<16)

FIG. 31

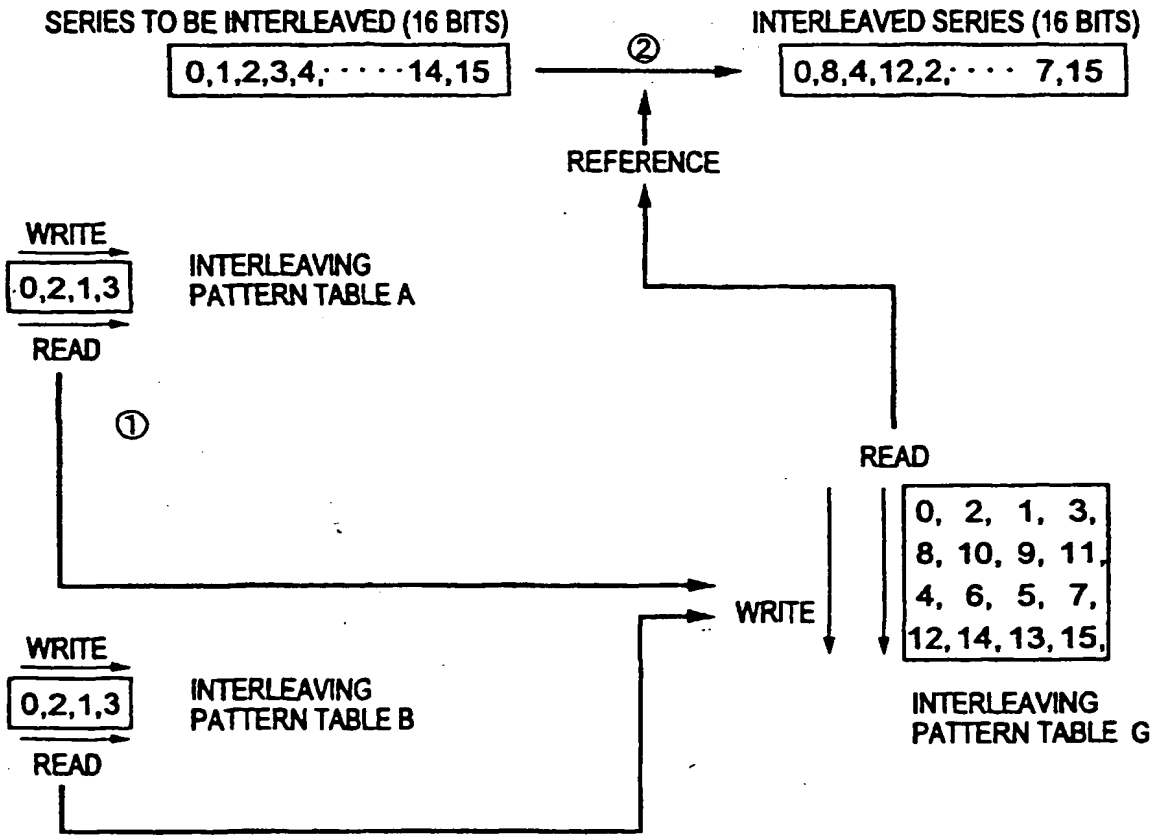

SERIES TO BE INTERLEAVED (16 BITS)
0,1,2,3,4,· · · ·14,15
②
INTERLEAVED SERIES (16 BITS)
0,8,4,12,2,· · · 7,15
REFERENCE
WRITE
0,2,1,3
READ
INTERLEAVING PATTERN TABLE A
①
READ
0, 2, 1, 3,
8, 10, 9, 11,
4, 6, 5, 7,
12, 14, 13, 15,
WRITE
WRITE
0,2,1,3
READ
INTERLEAVING PATTERN TABLE B
INTERLEAVING PATTERN TABLE G

FIG. 32

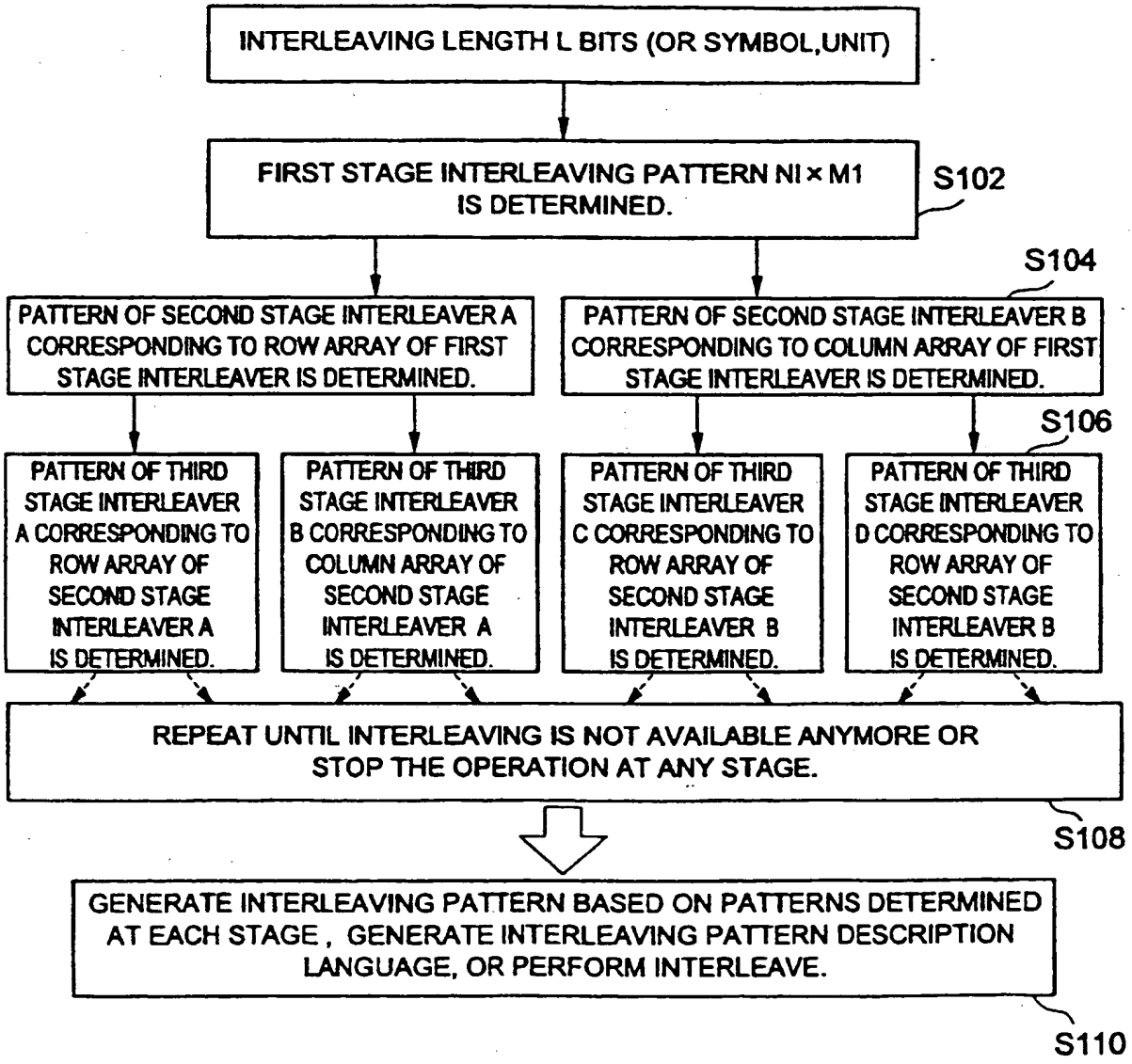

INTERLEAVING LENGTH L BITS (OR SYMBOL,UNIT)
FIRST STAGE INTERLEAVING PATTERN N1 × M1 IS DETERMINED.
S102
S104
PATTERN OF SECOND STAGE INTERLEAVER A CORRESPONDING TO ROW ARRAY OF FIRST STAGE INTERLEAVER IS DETERMINED.
PATTERN OF SECOND STAGE INTERLEAVER B CORRESPONDING TO COLUMN ARRAY OF FIRST STAGE INTERLEAVER IS DETERMINED.
S106
PATTERN OF THIRD STAGE INTERLEAVER A CORRESPONDING TO ROW ARRAY OF SECOND STAGE INTERLEAVER A IS DETERMINED.
PATTERN OF THIRD STAGE INTERLEAVER B CORRESPONDING TO COLUMN ARRAY OF SECOND STAGE INTERLEAVER A IS DETERMINED.
PATTERN OF THIRD STAGE INTERLEAVER C CORRESPONDING TO ROW ARRAY OF SECOND STAGE INTERLEAVER B IS DETERMINED.
PATTERN OF THIRD STAGE INTERLEAVER D CORRESPONDING TO ROW ARRAY OF SECOND STAGE INTERLEAVER B IS DETERMINED.
REPEAT UNTIL INTERLEAVING IS NOT AVAILABLE ANYMORE OR STOP THE OPERATION AT ANY STAGE.
S108
GENERATE INTERLEAVING PATTERN BASED ON PATTERNS DETERMINED AT EACH STAGE , GENERATE INTERLEAVING PATTERN DESCRIPTION LANGUAGE, OR PERFORM INTERLEAVE.
S110

FIG. 33

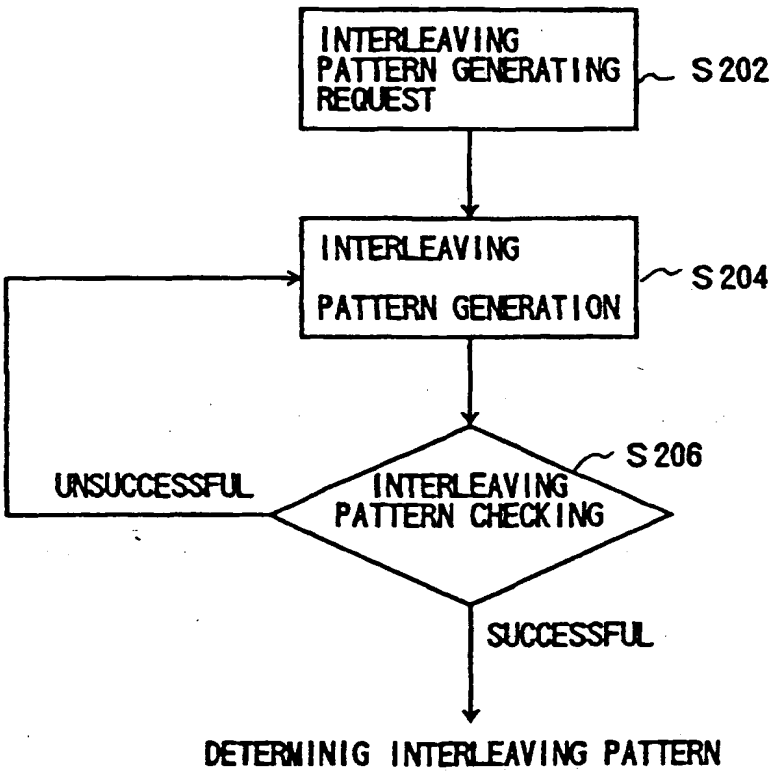
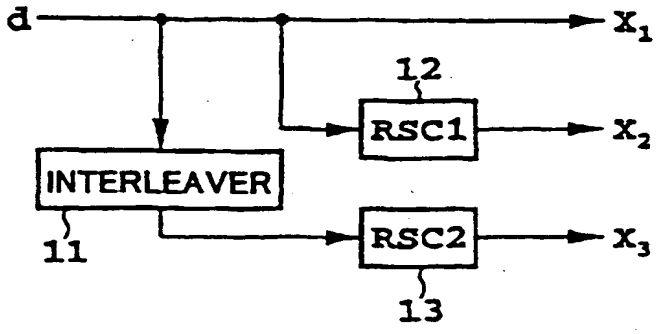

INTERLEAVING PATTERN GENERATING REQUEST
S202
INTERLEAVING PATTERN GENERATION
S204
S206
UNSUCCESSFUL
INTERLEAVING PATTERN CHECKING
SUCCESSFUL
DETERMINIG INTERLEAVING PATTERN

FIG. 34

(a)



(b)

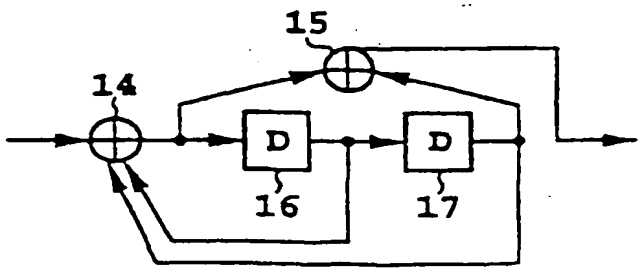


FIG. 35

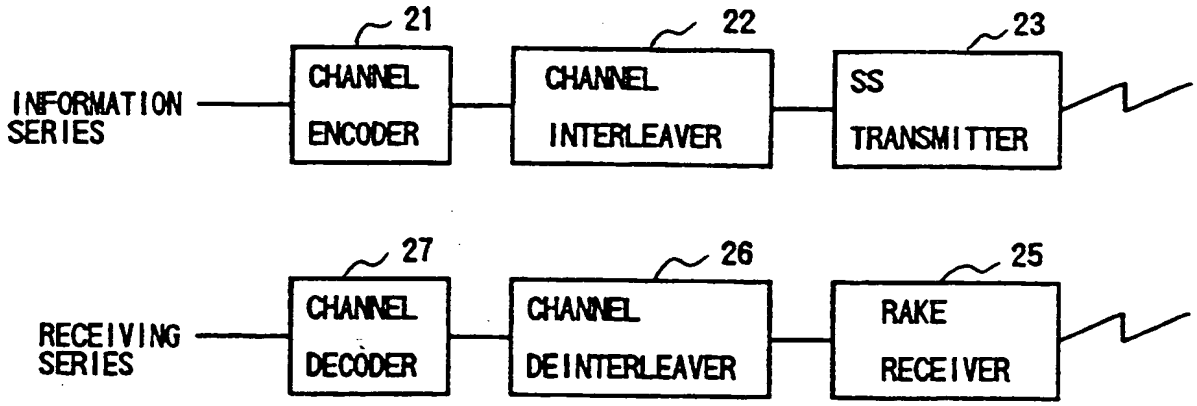

21
22
23
INFORMATION SERIES
CHANNEL ENCODER
CHANNEL INTERLEAVER
SS TRANSMITTER
27
26
25
RECEIVING SERIES
CHANNEL DECODER
CHANNEL DEINTERLEAVER
RAKE RECEIVER

FIG. 36

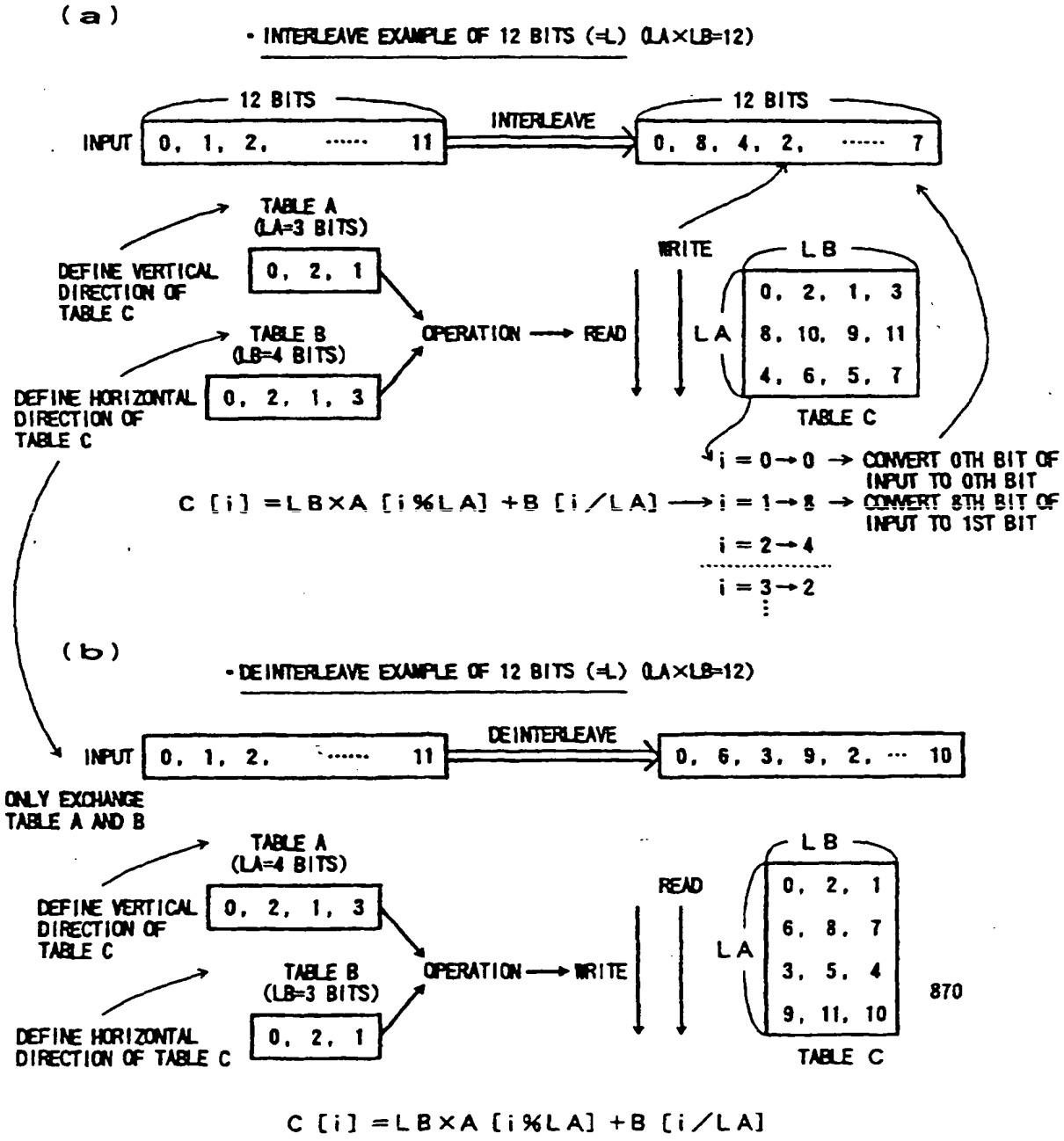
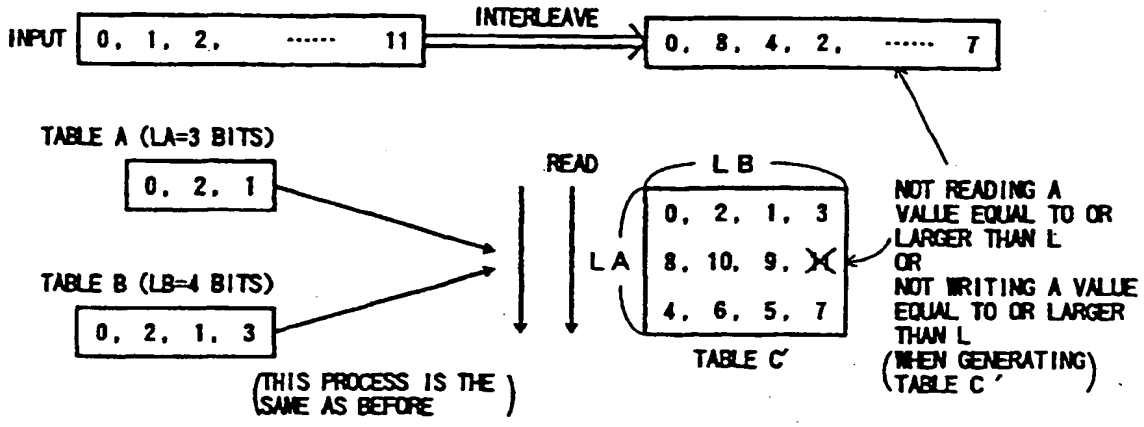

(a)
• INTERLEAVE EXAMPLE OF 12 BITS (=L) (LA×LB=12)
12 BITS
INPUT
0, 1, 2, ... 11
INTERLEAVE
12 BITS
0, 8, 4, 2, ... 7
TABLE A
(LA=3 BITS)
DEFINE VERTICAL DIRECTION OF TABLE C
0, 2, 1
TABLE B
(LB=4 BITS)
DEFINE HORIZONTAL DIRECTION OF TABLE C
0, 2, 1, 3
OPERATION
READ
WRITE
LB
LA
0, 2, 1, 3
8, 10, 9, 11
4, 6, 5, 7
TABLE C
C [i] =LB×A [i%LA] +B [i/LA]
i = 0→0 → CONVERT 0TH BIT OF INPUT TO 0TH BIT
i = 1→8 → CONVERT 8TH BIT OF INPUT TO 1ST BIT
i = 2→4
i = 3→2
(b)
• DEINTERLEAVE EXAMPLE OF 12 BITS (=L) (LA×LB=12)
INPUT
0, 1, 2, ... 11
DEINTERLEAVE
0, 6, 3, 9, 2, ··· 10
ONLY EXCHANGE TABLE A AND B
TABLE A
(LA=4 BITS)
DEFINE VERTICAL DIRECTION OF TABLE C
0, 2, 1, 3
TABLE B
(LB=3 BITS)
DEFINE HORIZONTAL DIRECTION OF TABLE C
0, 2, 1
OPERATION
WRITE
READ
LB
LA
0, 2, 1
6, 8, 7
3, 5, 4
9, 11, 10
TABLE C
870
C [i] =LB×A [i%LA] +B [i/LA]

FIG. 37

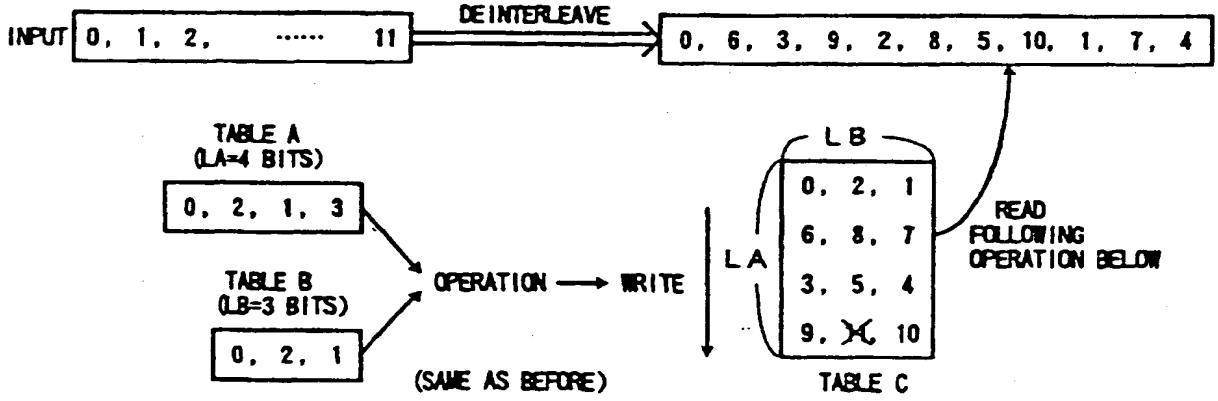
(a)

• INTERLEAVE EXAMPLE OF 11 BITS (=L) (LA×LB>L)



(b)

• DEINTERLEAVE EXAMPLE OF 11 BITS (=L) (LA×LB>L)



$$C[i] = LB \times A[i \% LA] + B[i / LA] - \alpha \quad (0 \leq i \leq (L-1))$$

α FOLLOWS FOLLOWING RULE

```
α = 0
for (j = 0, j < (LA×LB−L), j++) {
if C[i] >= LB×A[(L−1−j) %LA]
                +B[(L−1−j) /LA]
    α++;
}
```

FIG. 38

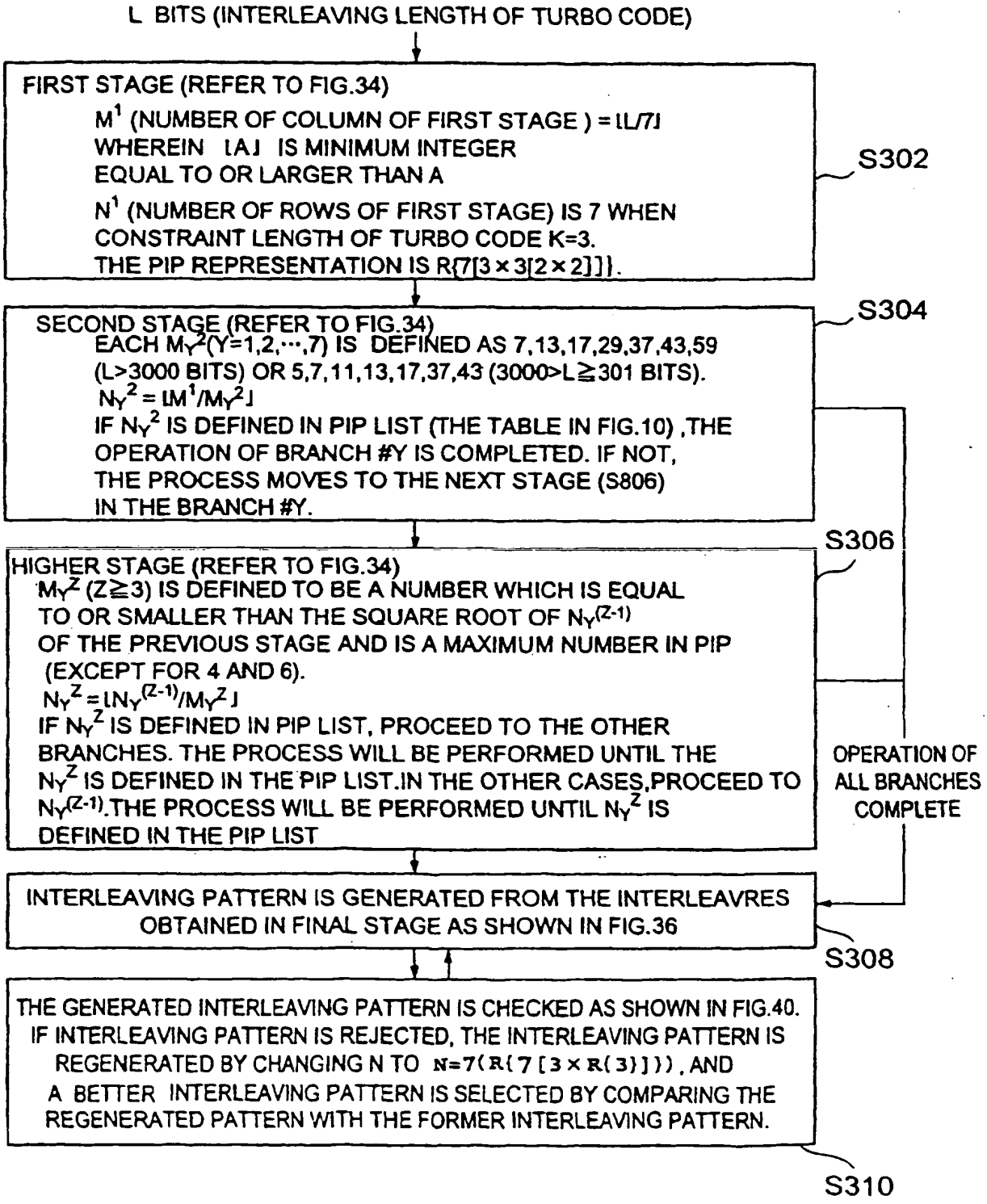
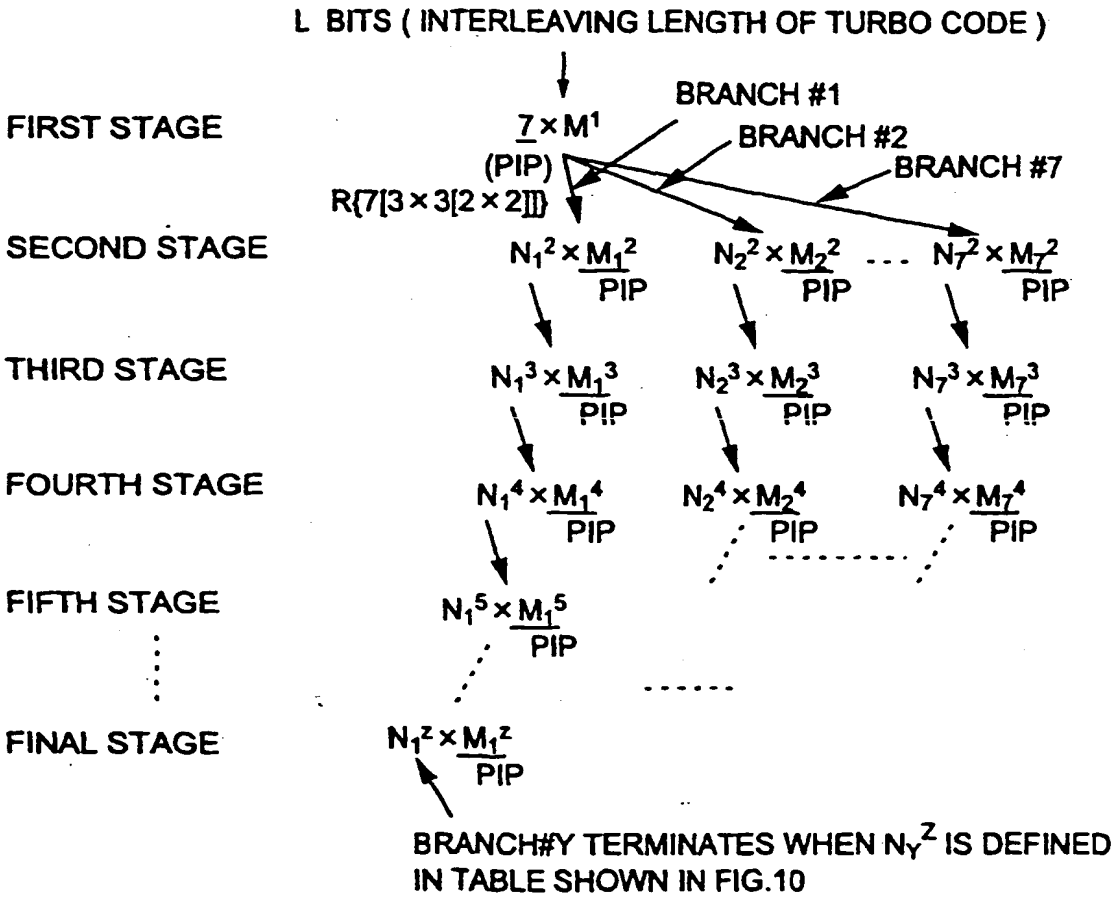

L BITS (INTERLEAVING LENGTH OF TURBO CODE)
FIRST STAGE (REFER TO FIG.34)
M1 (NUMBER OF COLUMN OF FIRST STAGE) = ⌊L/7⌋
WHEREIN ⌊A⌋ IS MINIMUM INTEGER EQUAL TO OR LARGER THAN A
N1 (NUMBER OF ROWS OF FIRST STAGE) IS 7 WHEN CONSTRAINT LENGTH OF TURBO CODE K=3.
THE PIP REPRESENTATION IS R{7[3×3[2×2]]}.
S302
SECOND STAGE (REFER TO FIG.34)
EACH MY2(Y=1,2,···,7) IS DEFINED AS 7,13,17,29,37,43,59 (L>3000 BITS) OR 5,7,11,13,17,37,43 (3000>L≧301 BITS).
NY2 = ⌊M1/MY2⌋
IF NY2 IS DEFINED IN PIP LIST (THE TABLE IN FIG.10) ,THE OPERATION OF BRANCH #Y IS COMPLETED. IF NOT, THE PROCESS MOVES TO THE NEXT STAGE (S806) IN THE BRANCH #Y.
S304
HIGHER STAGE (REFER TO FIG.34)
MYZ (Z≧3) IS DEFINED TO BE A NUMBER WHICH IS EQUAL TO OR SMALLER THAN THE SQUARE ROOT OF NY(Z-1) OF THE PREVIOUS STAGE AND IS A MAXIMUM NUMBER IN PIP (EXCEPT FOR 4 AND 6).
NYZ = ⌊NY(Z-1)/MYZ⌋
IF NYZ IS DEFINED IN PIP LIST, PROCEED TO THE OTHER BRANCHES. THE PROCESS WILL BE PERFORMED UNTIL THE NYZ IS DEFINED IN THE PIP LIST.IN THE OTHER CASES,PROCEED TO NY(Z-1).THE PROCESS WILL BE PERFORMED UNTIL NYZ IS DEFINED IN THE PIP LIST
S306
OPERATION OF ALL BRANCHES COMPLETE
INTERLEAVING PATTERN IS GENERATED FROM THE INTERLEAVRES OBTAINED IN FINAL STAGE AS SHOWN IN FIG.36
S308
THE GENERATED INTERLEAVING PATTERN IS CHECKED AS SHOWN IN FIG.40. IF INTERLEAVING PATTERN IS REJECTED, THE INTERLEAVING PATTERN IS REGENERATED BY CHANGING N TO N=7(R{7[3×R{3}]}), AND A BETTER INTERLEAVING PATTERN IS SELECTED BY COMPARING THE REGENERATED PATTERN WITH THE FORMER INTERLEAVING PATTERN.
S310

FIG.39



$$L[N^1\{PIP\}\times M^1[N_1{}^1[N_1{}^2[\cdots]\times M_1{}^2\{PIP\}\times M_1{}^1\{PIP\},\ N_2{}^1[\cdots]\times M_2{}^1\{PIP\},\ \cdots\cdots,\ N_7{}^1[\cdots]\times M_7{}^1\{PIP\}]$$

FIG. 40

index	EXPRESSION	INTERLEAVING PATTERN
T7	R{7[3×3[2×2]]}	4,1,5,2,6,3,0
T7'	R{7[3×R{3}]}	6,3,0,4,1,5,2
2	R{2}	1,0
3	R{3[2×2]}	1,2,0
4	4[2×R{2}]	1,3,0,2
5	5[2×3]	0,3,1,4,2
6	6[3×2]	0,2,4,1,3,5
7	7[3×3[2×2]]	0,3,6,2,5,1,4
8	8[4[2×2]×2]	0,4,2,6,1,5,3,7
9	9[R{2}×5[2×3]]	5,0,8,3,6,1,4,7,2
11	11[3×5[3×2]]	0,5,10,2,7,4,9,1,6,3,8
13	13[2×7[3×3[2×2],3[2×2,2×R{2},2×R{2}]×3{R{3}×1,R{3}×1,3×1}]]	0,9,3,12,6,2,11,5,8,1,10,4,7
17	17[4[2×2,4×1,4×1,4×1]×5[3×2]]	0,10,5,15,2,7,12,4,9,14,1,6,11,16,3,8,13
20	20[4[2×R{2}]×5[2×3]]	5,15,0,10,8,18,3,13,6,16,1,11,9,19,4,14,7,17,2,12
29	29[5[3×2]×7[3×3[2×2]]]	0,14,28,7,21,3,17,10,24,6,20,13,27,2,16,9,23,5,19,12,26,1,15,8,22,4,18,11,25
37	37[7[3×3]×6[3×2]]	0,18,36,6,24,12,30,2,20,8,26,14,32,4,22,10,28,16,34,1,19,7,25,13,31,3,21,9,27,15,33,5,23,11,29,17,35
43	43[4[2×2]×11[3×5[3×2]]]	0,22,11,33,5,27,16,38,10,32,21,2,24,13,35,7,29,18,40,4,26,15,37,9,31,20,42,1,23,12,34,6,28,17,39,3,25,14,36,8,30,19,41
47	47[7[3×3]×7[3×3]]	0,21,42,7,28,14,35,3,24,45,10,31,17,38,6,27,13,34,20,41,1,22,43,8,29,15,36,4,25,46,11,32,18,39,2,23,44,9,30,16,37,5,26,12,33,19,40
53	53[5[2×3]×11[3×5[3×2]]]	0,33,11,44,22,5,38,16,49,27,10,43,21,32,2,35,13,46,24,7,40,18,51,29,4,37,15,48,26,9,42,20,31,1,34,12,45,23,6,39,17,50,28,3,36,14,47,25,8,41,19,52,30
59	59[9[R{2}×5[2×3]]×7[3×3]]	35,0,56,21,42,7,28,49,14,38,3,24,45,10,31,52,17,41,6,27,48,13,34,55,20,36,1,57,22,43,8,29,50,15,39,4,25,46,11,32,53,18,37,2,58,23,44,9,30,51,16,40,5,26,47,12,33,54,19
61	61[5[2×3]×13[5[2×3]×3[2×2]]]	0,39,13,52,26,9,48,22,35,3,42,16,55,29,12,51,25,38,6,45,19,58,32,2,41,15,54,28,11,50,24,37,5,44,18,57,31,8,47,21,60,34,1,40,14,53,27,10,49,23,36,4,43,17,56,30,7,46,20,59,33

FIG.41

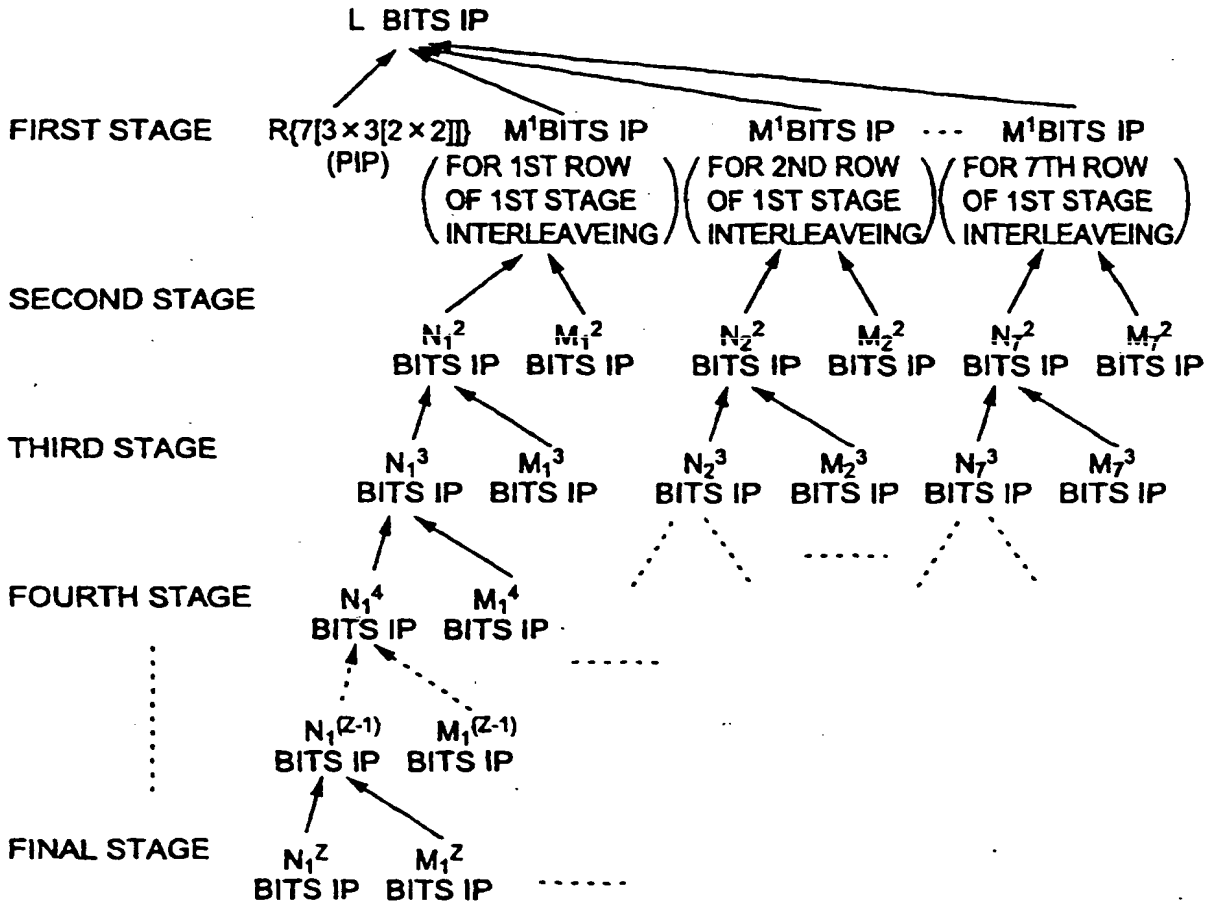

L BITS IP
FIRST STAGE
R{7[3×3[2×2]]}
(PIP)
M¹BITS IP
FOR 1ST ROW OF 1ST STAGE INTERLEAVEING
M¹BITS IP
FOR 2ND ROW OF 1ST STAGE INTERLEAVEING
M¹BITS IP
FOR 7TH ROW OF 1ST STAGE INTERLEAVEING
SECOND STAGE
N1² BITS IP
M1² BITS IP
N2² BITS IP
M2² BITS IP
N7² BITS IP
M7² BITS IP
THIRD STAGE
N1³ BITS IP
M1³ BITS IP
N2³ BITS IP
M2³ BITS IP
N7³ BITS IP
M7³ BITS IP
FOURTH STAGE
N1⁴ BITS IP
M1⁴ BITS IP
N1(Z-1) BITS IP
M1(Z-1) BITS IP
FINAL STAGE
N1Z BITS IP
M1Z BITS IP

FIG.42

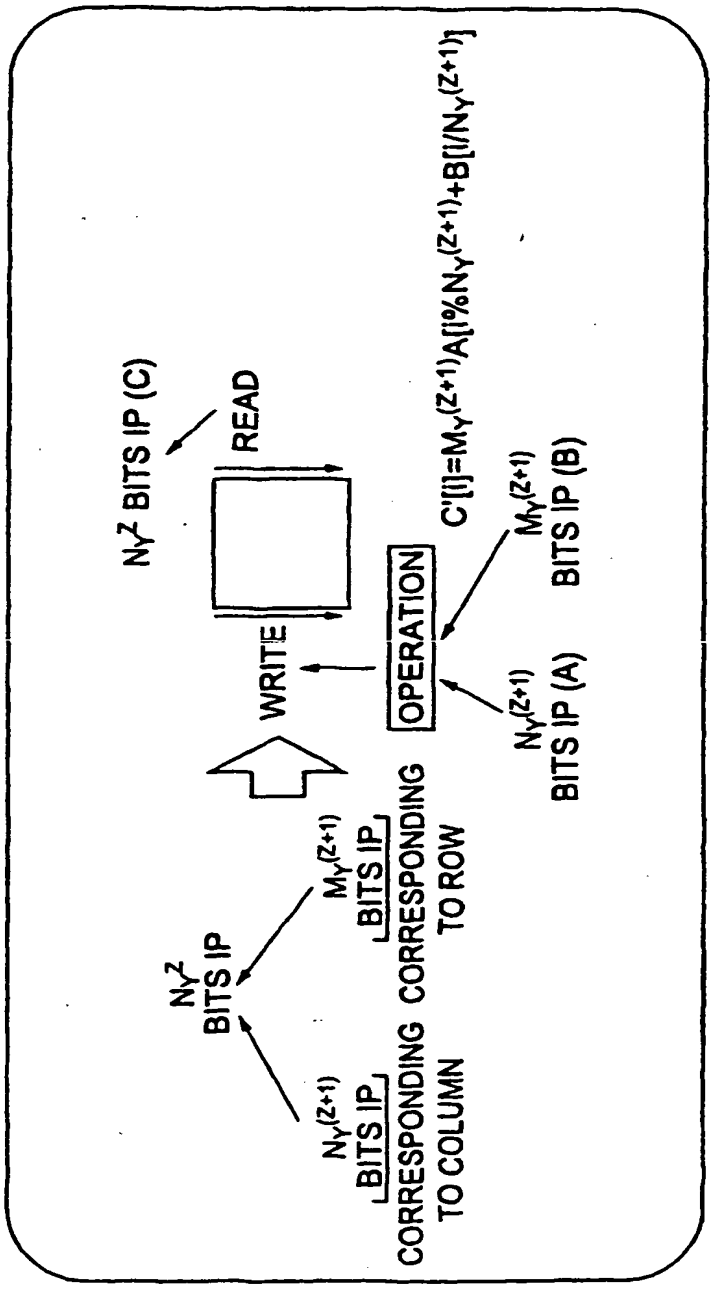

N_Y^Z BITS IP (C)
READ
WRITE
OPERATION
C'[I]=$M_Y^{(Z+1)}$A[I%$N_Y^{(Z+1)}$+B[I/$N_Y^{(Z+1)}$]
$M_Y^{(Z+1)}$ BITS IP (B)
$N_Y^{(Z+1)}$ BITS IP (A)
N_Y^Z BITS IP
$M_Y^{(Z+1)}$ BITS IP CORRESPONDING TO ROW
$N_Y^{(Z+1)}$ BITS IP CORRESPONDING TO COLUMN

FIG.43

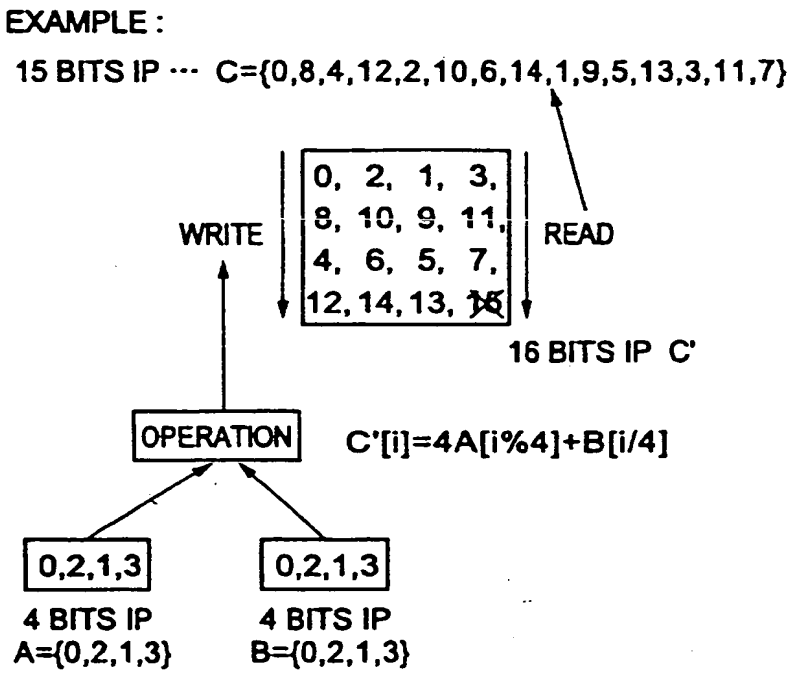

EXAMPLE :
15 BITS IP ··· C={0,8,4,12,2,10,6,14,1,9,5,13,3,11,7}
WRITE
0, 2, 1, 3,
8, 10, 9, 11,
4, 6, 5, 7,
12, 14, 13, 15
READ
16 BITS IP C'
OPERATION
C'[i]=4A[i%4]+B[i/4]
0,2,1,3
0,2,1,3
4 BITS IP
A={0,2,1,3}
4 BITS IP
B={0,2,1,3}

FIG.44

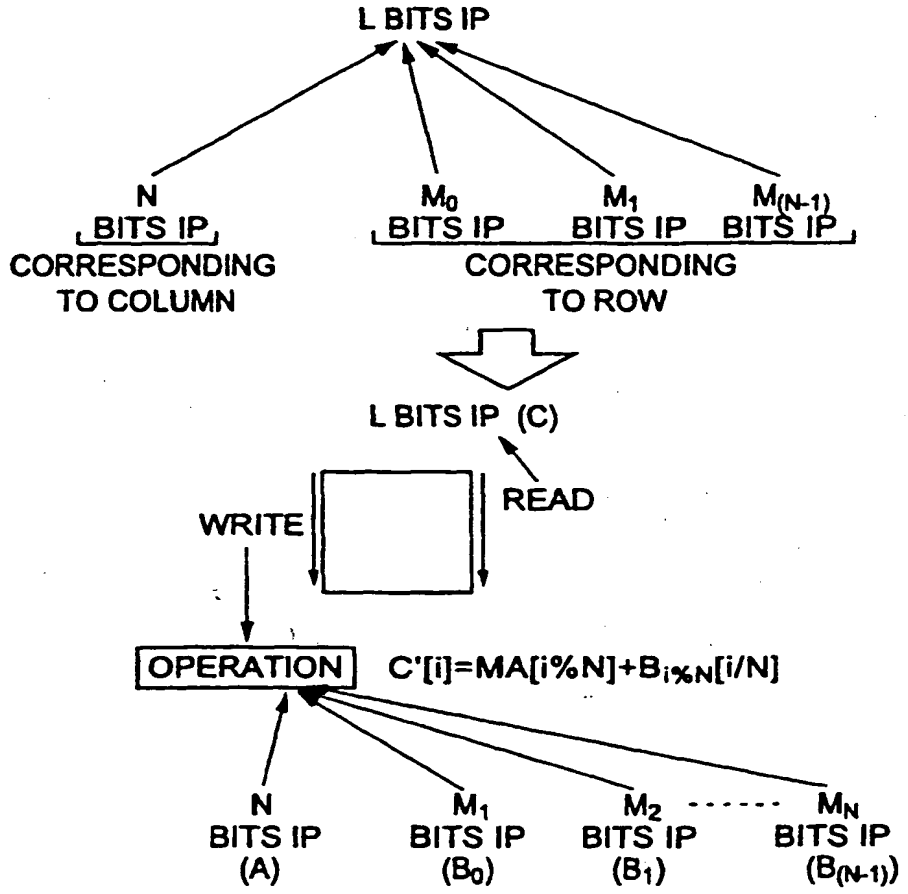

L BITS IP
N BITS IP CORRESPONDING TO COLUMN
M0 BITS IP
M1 BITS IP
M(N-1) BITS IP
CORRESPONDING TO ROW
L BITS IP (C)
READ
WRITE
OPERATION
C'[i]=MA[i%N]+Bi%N[i/N]
N BITS IP (A)
M1 BITS IP (B0)
M2 BITS IP (B1)
MN BITS IP (B(N-1))

FIG. 45

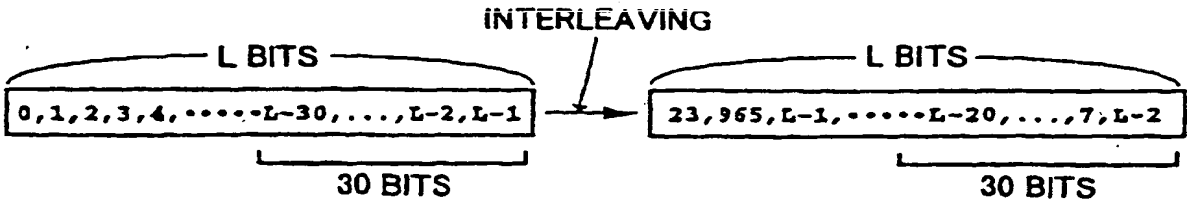

INTERLEAVING
L BITS
0,1,2,3,4,••••L-30,...,L-2,L-1
30 BITS
L BITS
23,965,L-1,••••L-20,...,7,L-2
30 BITS

FIG.46

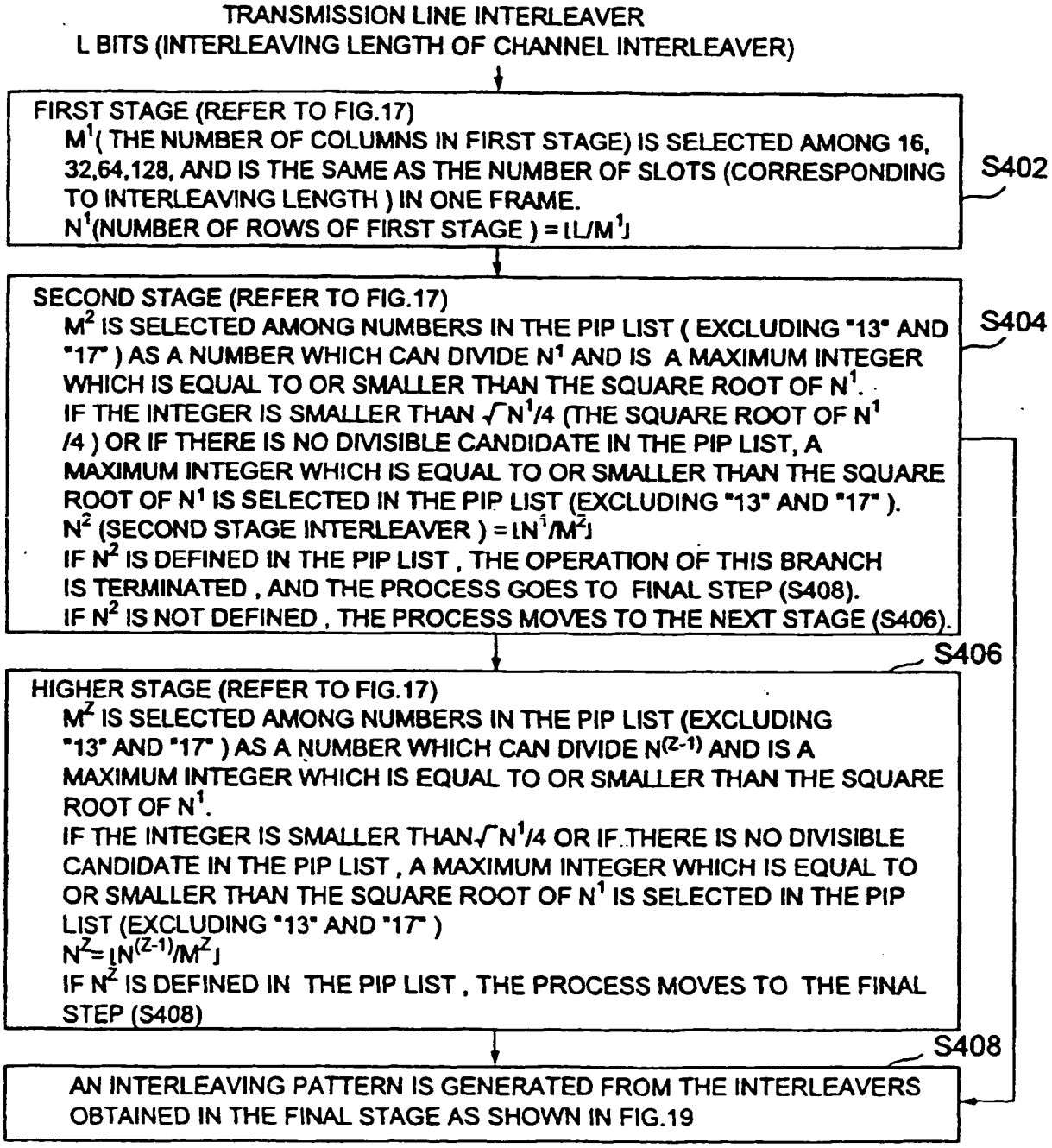

TRANSMISSION LINE INTERLEAVER
L BITS (INTERLEAVING LENGTH OF CHANNEL INTERLEAVER)
FIRST STAGE (REFER TO FIG.17)
M1(THE NUMBER OF COLUMNS IN FIRST STAGE) IS SELECTED AMONG 16, 32,64,128, AND IS THE SAME AS THE NUMBER OF SLOTS (CORRESPONDING TO INTERLEAVING LENGTH) IN ONE FRAME.
N1(NUMBER OF ROWS OF FIRST STAGE) = ⌊L/M1⌋
S402
SECOND STAGE (REFER TO FIG.17)
M2 IS SELECTED AMONG NUMBERS IN THE PIP LIST (EXCLUDING "13" AND "17") AS A NUMBER WHICH CAN DIVIDE N1 AND IS A MAXIMUM INTEGER WHICH IS EQUAL TO OR SMALLER THAN THE SQUARE ROOT OF N1.
IF THE INTEGER IS SMALLER THAN √N1/4 (THE SQUARE ROOT OF N1 /4) OR IF THERE IS NO DIVISIBLE CANDIDATE IN THE PIP LIST, A MAXIMUM INTEGER WHICH IS EQUAL TO OR SMALLER THAN THE SQUARE ROOT OF N1 IS SELECTED IN THE PIP LIST (EXCLUDING "13" AND "17").
N2 (SECOND STAGE INTERLEAVER) = ⌊N1/M2⌋
IF N2 IS DEFINED IN THE PIP LIST , THE OPERATION OF THIS BRANCH IS TERMINATED , AND THE PROCESS GOES TO FINAL STEP (S408).
IF N2 IS NOT DEFINED , THE PROCESS MOVES TO THE NEXT STAGE (S406).
S404
S406
HIGHER STAGE (REFER TO FIG.17)
MZ IS SELECTED AMONG NUMBERS IN THE PIP LIST (EXCLUDING "13" AND "17") AS A NUMBER WHICH CAN DIVIDE N(Z-1) AND IS A MAXIMUM INTEGER WHICH IS EQUAL TO OR SMALLER THAN THE SQUARE ROOT OF N1.
IF THE INTEGER IS SMALLER THAN√N1/4 OR IF THERE IS NO DIVISIBLE CANDIDATE IN THE PIP LIST , A MAXIMUM INTEGER WHICH IS EQUAL TO OR SMALLER THAN THE SQUARE ROOT OF N1 IS SELECTED IN THE PIP LIST (EXCLUDING "13" AND "17")
NZ= ⌊N(Z-1)/MZ⌋
IF NZ IS DEFINED IN THE PIP LIST , THE PROCESS MOVES TO THE FINAL STEP (S408)
S408
AN INTERLEAVING PATTERN IS GENERATED FROM THE INTERLEAVERS OBTAINED IN THE FINAL STAGE AS SHOWN IN FIG.19

FIG.47

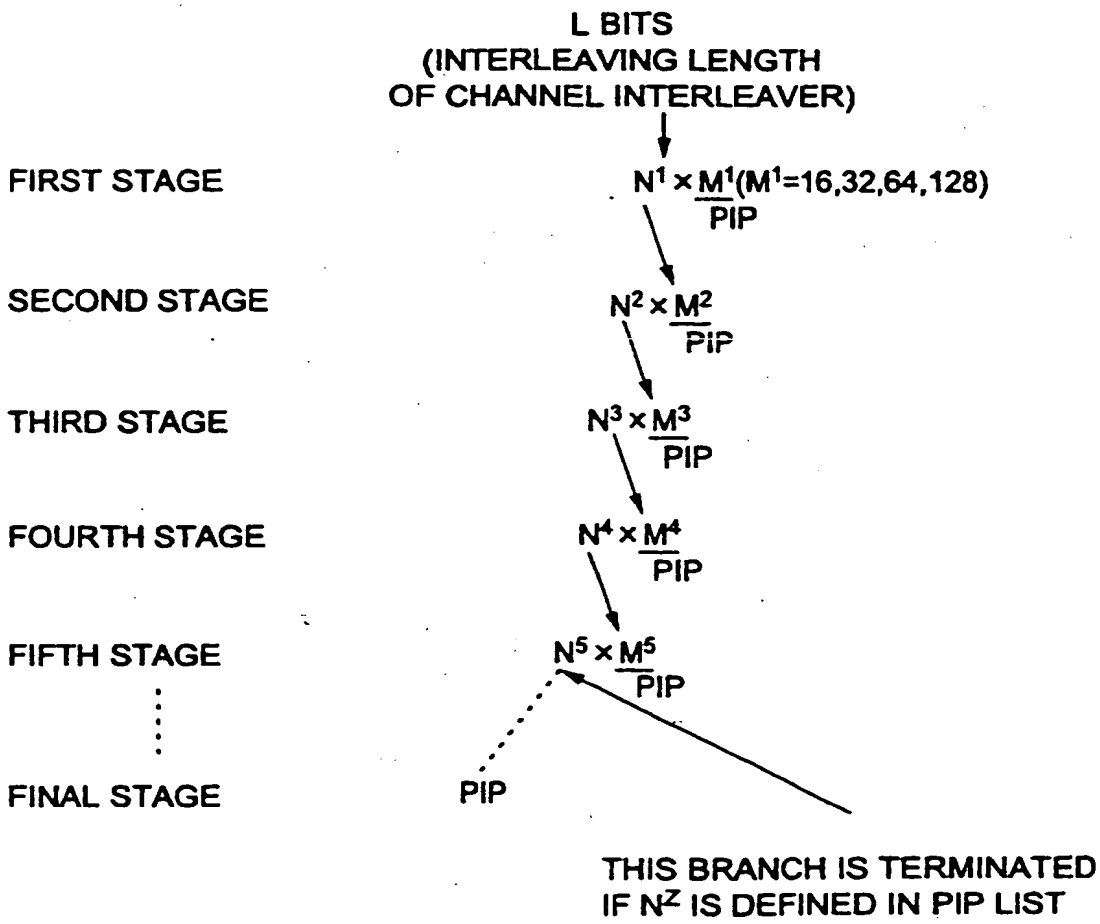

L BITS
(INTERLEAVING LENGTH
OF CHANNEL INTERLEAVER)
FIRST STAGE
SECOND STAGE
THIRD STAGE
FOURTH STAGE
FIFTH STAGE
FINAL STAGE
N1 × M1/PIP (M1=16,32,64,128)
N2 × M2/PIP
N3 × M3/PIP
N4 × M4/PIP
N5 × M5/PIP
PIP
THIS BRANCH IS TERMINATED
IF NZ IS DEFINED IN PIP LIST

FIG. 48.

index	EXPRESSION	INTERLEAVING PATTERN
2	2	0,1
3	3	0,1,2
4	4[2×2]	0,2,1,3
5	5[2×3]	0,3,1,4,2
6	6[3×2]	0,2,4,1,3,5
7	7[3×3[2×2]]	0,3,6,2,5,1,4
8	8[4[2×2]×2]	0,4,2,6,1,5,3,7
9	9[3×3]	0,3,6,1,4,7,2,5,8
10	10[5[3×2]×2]	0,4,8,2,6,1,5,9,3,7
11	11[3×5[3×2]]	0,5,10,2,7,4,9,1,6,3,8
13	13[2×7[3×3[2×2],3[2×2,2×R{2},2×R{2}]×3[R{3}×1,R{3}×1,3×1]]]	0,9,3,12,6,2,11,5,8,1,10,4,7
16	16[4[2×2]×4[2×2]]	0,8,4,12,2,10,6,14,1,9,5,13,3,11,7,15
17	17[4[2×2,4×1,4×1,4×1,4×1]×5[3×2]]	0,10,5,15,2,7,12,4,9,14,1,6,11,16,3,8,13
20	20[4[2×2]×5[3×2]]	0,10,5,15,2,12,7,17,4,14,9,19,1,11,6,16,3,13,8,18
32	32[8[4[2×2]×2]×4[2×2]]]	0,16,8,24,4,20,12,28,2,18,10,26,6,22,14,30,1,17,9,25,5,21,13,29,3,19,11,27,7,23,15,31
64	64[8[4[2×2]×2]×8[4[2×2]×2]]	0,32,16,48,8,40,24,56,4,36,20,52,12,44,28,60,2,34,18,50,10,42,26,58,6,38,22,54,14,46,30,62,1,33,17,49,9,41,25,57,5,37,21,53,13,45,29,61,3,35,19,51,11,43,27,59,7,39,23,55,15,47,31,63
128	128[16[4[2×2]×4[2×2]]×8[4[2×2]×2]]	0,64,32,96,16,80,48,112,8,72,40,104,24,88,56,120,4,68,36,100,20,84,52,116,12,76,44,108,28,92,60,124,2,66,34,98,18,82,50,114,10,74,42,106,26,90,58,122,6,70,38,102,22,86,54,118,14,78,46,110,30,94,62,126,1,65,33,97,17,81,49,113,9,73,41,105,25,89,57,121,5,69,37,101,21,85,53,117,13,77,45,109,29,93,61,125,3,67,35,99,19,83,51,115,11,75,43,107,27,91,59,123,7,71,39,103,23,87,55,119,15,79,47,111,31,95,63,127

FIG.49

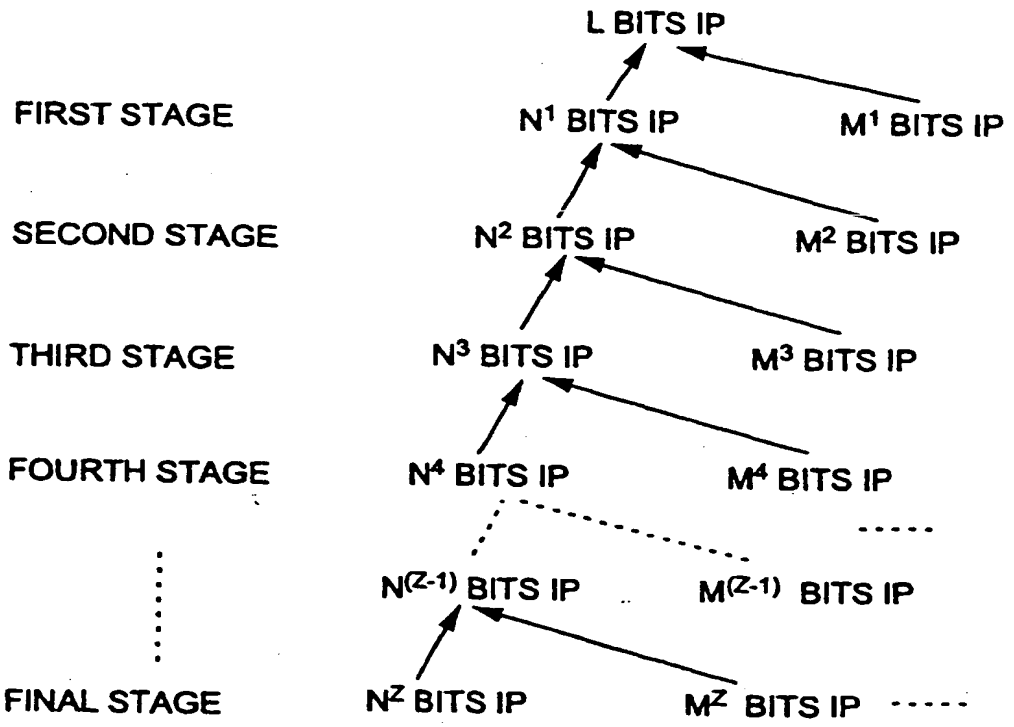
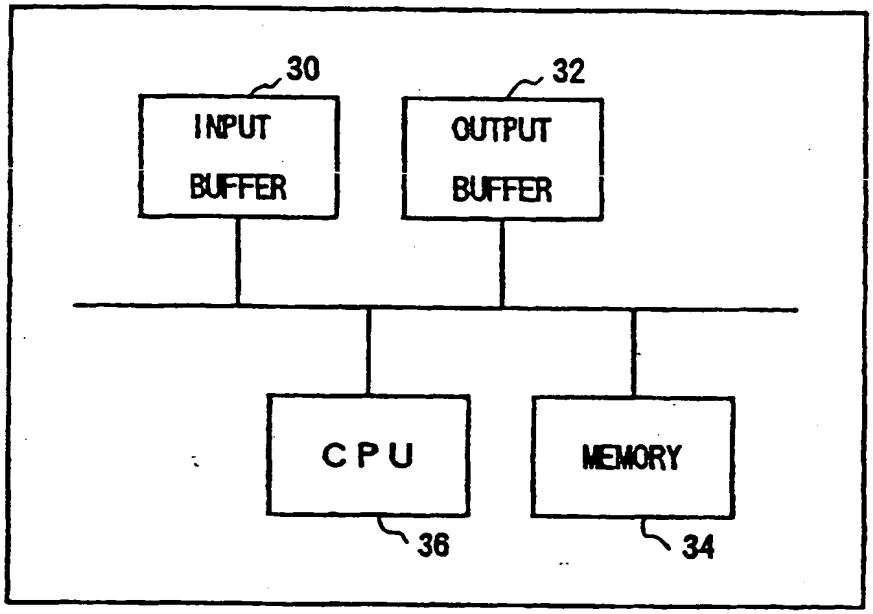

L BITS IP
FIRST STAGE
N1 BITS IP
M1 BITS IP
SECOND STAGE
N2 BITS IP
M2 BITS IP
THIRD STAGE
N3 BITS IP
M3 BITS IP
FOURTH STAGE
N4 BITS IP
M4 BITS IP
N(Z-1) BITS IP
M(Z-1) BITS IP
FINAL STAGE
NZ BITS IP
MZ BITS IP

FIG. 50



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP98/05027

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[6] H03M13/22, H03M13/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[6] H03M13/00-13/22

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1996 Toroku Jitsuyo Shinan Koho 1994-1999
Kokai Jitsuyo Shinan Koho 1971-1999 Jitsuyo Shinan Toroku Koho 1996-1999

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	S. Dolinar and D. Divsalar, "Weight Distributions for Turbo Codes Using Random and Nonrandom Permutations", The Telecommunications and Data Acquisition Report (JPL TDA Progress Report) 42-122, Jet Propulsion Laboratory, August 15, 1995, Pasadena, California, pp.56-65, Particularly refer to Section IV.B.1 (page 61, lines 33 to 48)	1-4 6, 26, 27, 29 28
X Y A	JP, 07-212250, A (Fujitsu Ltd.), 11 August, 1995 (11. 08. 95) (Family: none) Particularly refer to Fig. 4	5 6, 26, 27, 29 28
X A	S.V. Maric, "Class of algebraically constructed permutations for use in pseudorandom interleavers", Electronics Letters, Vol. 30, No. 17, 18th August 1994, pp.1378-1379, particularly refer to "It is common ··· permuted sequence." (page 1378, right column, lines 50 to 53)	7-18 21-25, 28, 30-34

[x] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 January, 1999 (27. 01. 99)	9 February, 1999 (09. 02. 99)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP98/05027

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	P. Jung and M. Nasshan, "Performance evaluation of turbo codes for short frame transmission systems", Electronics Letters, Vol. 30, No. 2, 20th January 1994, pp.111-113, particularly refer to page 112, left column, lines 23 to 49	19, 20
X	JP, 08-242217, A (AT&T Corp.), 17 September, 1996 (17. 09. 96) & EP, 715432, A2 & US, 5659580, A & CN, 1132453, A Particularly refer to Par. Nos. [0019], [0020]	7
X	JP, 08-97731, A (Sony Corp.), 12 April, 1996 (12. 04. 96) (Family: none) Particularly refer to page 1, abstract	7
A	JP, 07-30846, A (Hitachi,Ltd.), 31 January, 1995 (31. 01. 95) (Family: none) Particularly refer to Figs. 1, 2	1-34
A	JP, 55-26715, A (Kokusai Denshin Denwa Co., Ltd.), 26 February, 1980 (26. 02. 80) (Family: none) Particularly refer to Fig. 5	1-34
A	JP, 10-98397, A (Fujitsu General Ltd.), 14 April, 1998 (14. 04. 98) (Family: none)	1-34
A	E. Dunscombe and F.C. Piper, "Optimal Interleaving Scheme for Convolutional Codes", Electronics Letters, Vol. 25, No. 22, 26th October 1989, pp.1517-1518, particularly refer to abstract	1-34
P, X P, A	Akira Shibuya, Hiroto Suda, Fumiyuki Adachi, "Effect of Application of Multi-Interleaving Method to W-CDMA (in Japanese)", IEICE, Technical Report, Vol. 97, No. 544, A·P97-178, 18 February, 1998 (18. 02. 98), pp.23-30 Particularly refer to Section 2 (page 24, right column, line 1 to page 25, right column, line 24), Section 3.3.2 (page 27, left column, line 11 to right column, line 20)	1-4 5-34

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